HybridPACK™

Hybrid Kit for HybridPACK™2

Evaluation Kit for Applications with HybridPACK™2 Module

Application Note

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System Engineering

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Hybrid Kit for HybridPACK™2

Revision History: 2014-08-11, V2.4

Previous Revision: V2.3

Page	Subjects (major changes since last revision)
36	**Figure 29**, changed capacitors C875 (from 22uF to 4.5uF) and C876 (from 22uF to 100uF)
48	**Figure 3**, changed capacitors C875 (from 22uF to 4.5uF) and C876 (from 22uF to 100uF)

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1 Introduction

The **Hybrid Kit for HybridPACK™2** shown in **Figure 1** was developed to support customers during their first steps in designing applications with **HybridPACK™2** IGBT module. The following chapters provide a detailed description of the main components and their functionality. This information is intended to enable the customers to re-use and modify the original Hybrid Kit design and qualify their own design for the production, according to their own specific requirements.

The boards **Hybrid Kit for HybridPACK™2 Evaluation Driver Board** (further referred as **"Driver Board"**) and **Hybrid Kit for HybridPACK™2 Logic Board** (further referred as **"Logic Board"**) provided by Infineon Technologies are subjected to functional testing only.

The current implementation of the **Hybrid Kit for HybridPACK™2** (e.g. electrical schematics) is **for reference only!** It does not cover in general all application specific requirements. **For specific recommendations** on how to implement designs with **HybridPACK™2** and **EiceDRIVER™**, please contact your local Infineon sales partner. More information is available on www.infineon.com.

Due to their purpose the system is not subjected to the same procedures regarding Returned Material Analysis (RMA), Process Change Notification (PCN) and Product Withdraw (PWD) as regular products.

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1.1 How to Order Hybrid Kit for HybridPACK™2

Hybrid Kit for HybridPACK™2 and **Hybrid Kit for HybridPACK™2 Evaluation Driver Board** (that can be ordered separately) have Infineon Technologies SAP numbers and can be ordered via Infineon Sales Partners.

- SAP ordering number for Hybrid Kit for HybridPACK™2: **SP000635950**
- SAP ordering number for Hybrid Kit for HybridPACK™2 Evaluation Driver Board: **SP000552868**

Information can also be found at the Infineon Technologies web page: www.infineon.com

Figure 1 The Hybrid Kit for HybridPACK™2

W A R N I N G !

Please always take care of the dead-time settings of the driver (to avoid short circuit conditions on the IGBT module) and always have on mind that Hybrid Kit for HybridPACK™2 inverter has no breaking chopper or similar hardware protection to absorb the energy generated during the regenerative breaking of a motor. In any case user shall ensure that voltage, current and temperature are monitored properly, e.g. by software or additional supporting hardware.

2 Design Features

The Hybrid Kit for HybridPACK™2 is made up of two PCBs (Driver Board and Logic Board) mechanically and electrically suitable to be used with an IGBT Module HybridPACK™2 (included), a DC-bus capacitor and a cooler. All these components build a complete main inverter for (H)EV applications up to 80kW.

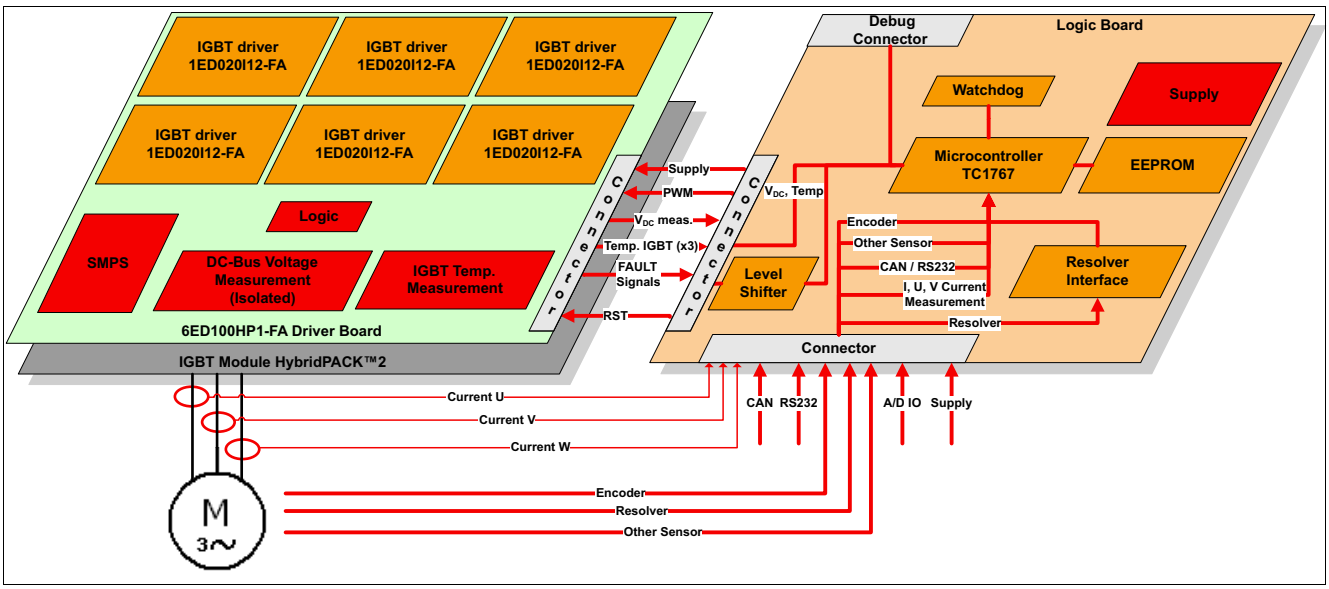


Figure 2 Block Diagram of Hybrid Kit for HybridPACK™2

Figure 2 show the complete block diagram for the system and the following sections provide an overview of the single components including main features, key data, pin assignments and mechanical dimensions.

2.1 Main Features

- Complete main inverter for (H)EV applications up to 80kW
- Automotive qualified IGBT module HybridPACK™2
  - 650V/800A IGBT & Diode chipset
- Automotive qualified Driver IC 1ED020I12-FA
  - Based on coreless transformer technology
  - Up to 1200V and 2A driving capability
  - $V_{CE\ sat}$ - detection
- TriCore™ family 32-bit microcontroller TC1767: member of the AUDO FUTURE product family designed for automotive applications
- Possibility of usage of different motor position interfaces: encoder, resolver, GMR (Giant Magneto-Resistance) or hall sensor

2.2 Dimensions

Figure 3 shows the dimensions of a complete Hybrid Kit for HybridPACK™2.

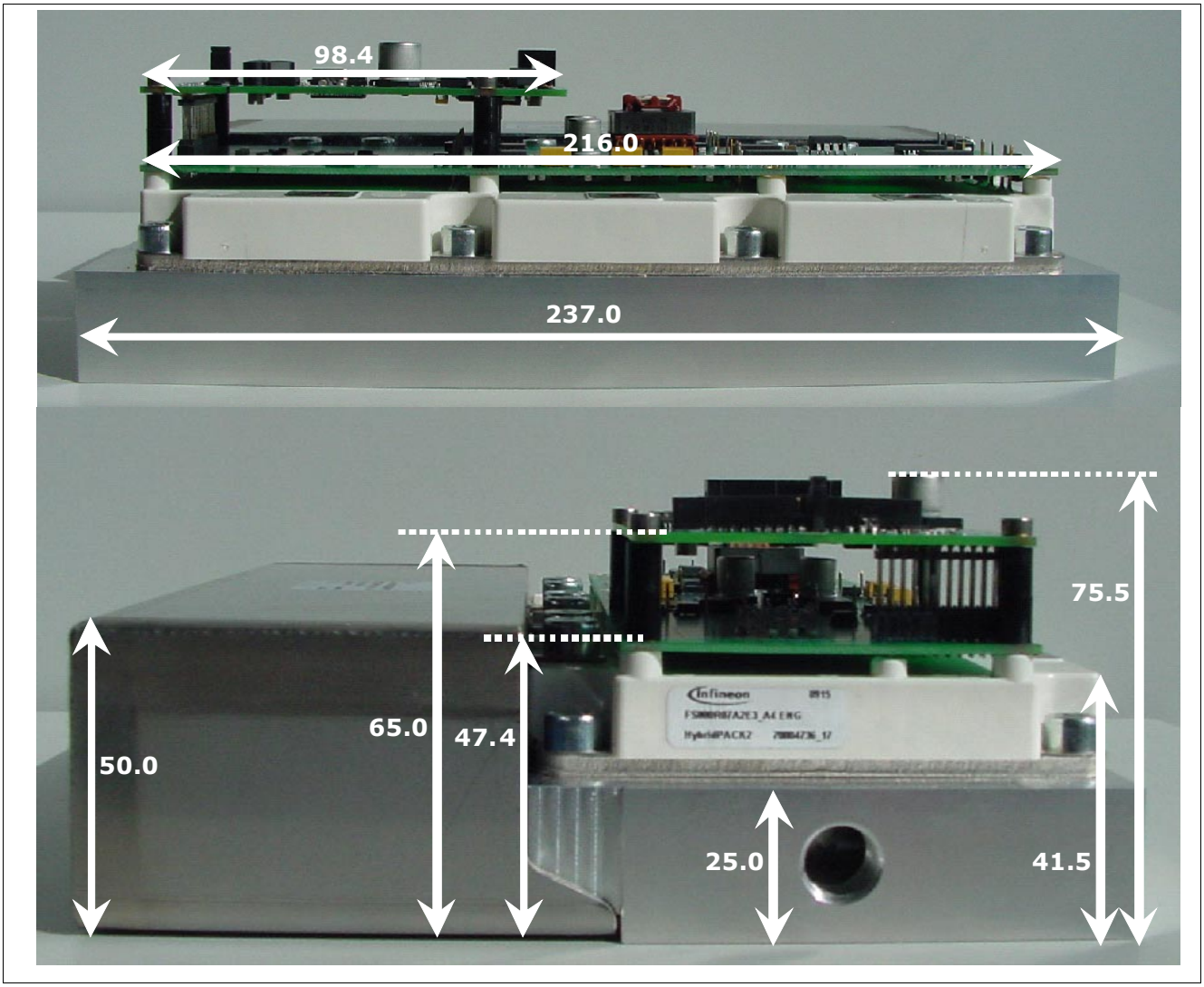


Figure 3 Dimensions of the Hybrid Kit for HybridPACK™2 (all dimensions are in mm)

Remark: Logic Board v1.3b is 2mm longer than Logic Board v1.2 (100.4 mm comparing to 98.4 mm).

2.3 Key Components

For detailed technical information about the different components please refer to the different web pages on the Infineon Internet.

2.3.1 Driver Board (6ED100HP2-FA)

The 6ED100HP2-FA is a six channel IGBT driver board, specially designed for the HybridPACK™2 IGBT module. The main features and a detailed description of the board, including schematics and layout, can be found in **Chapter 3**.

2.3.2 Logic Board

The Logic Board contains all necessary components for the control of the system. Furthermore it offers the connections to the motor positioning system (encoder, resolver or GMR) and to the current measurement system. For a detailed description of the board please refer to **Chapter 3**.

2.3.3 HybridPACK™2

(see **Figure 4**) is a power module designed for Full Hybrid Electrical Vehicle (HEV) applications for a power range up to 80kW. Designed for a junction operation temperature at 150°C, the module accommodates a six-pack configuration of 3rd generation Trench-Field-Stop IGBT and matching emitter controlled diodes and is rated up to 800A/650V. It is based on Infineon Technologies leading TRENCHSTOP™ IGBT Technology, which offers lowest conduction and switching losses.

HybridPACK™2 is designed for direct water-cooled inverter systems (temperature of coolant 75°C). The Pin Fin copper base plate combined with high-performance ceramic substrate and Infineon Technologies enhanced wire-bonding process provides unparalleled thermal cycling and power cycling reliability for full hybrid inverter applications. For a compact inverter design the driver stage PCB can easily be soldered on top of the module. All power connections are realized with screw terminals.

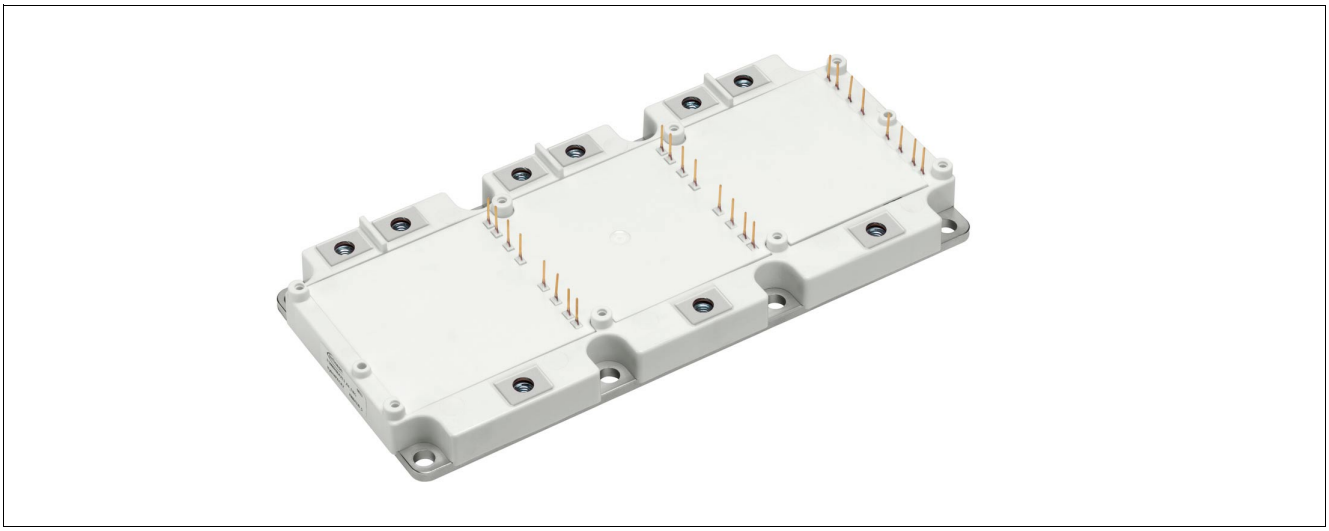


Figure 4 HybridPACK™2 IGBT Six-Pack Module

2.3.4 DC-Link Capacitors

For Hybrid Kit for HybridPACK™2 are used Epcos B25655J4507K and Kemet C4EEGMX6500AAUK as DC bus capacitors.

2.3.4.1 EPCOS B25655J4507K

The main features of the power electronic capacitor B25655J4507K from Epcos AG (see **Figure 5**) are shown in **Table 1**. Please refer to the Epcos datasheet for further details.

Table 1 Key Data of DC-Link Capacitor

Characteristics		Maximum ratings		Test Data	
C_R	500 µF ±10%	V_s	600V	V_{TT}	675V DC, 10s
V_R	450V DC	î	2kA	R_{ins} ·C	≥ 10000s
W_R	50Ws	I_s	8kA	tan δ (50 Hz)	≤ $8 \cdot 10^{-4}$
I_{max}	120A	$(dV/dt)_{max}$	4V/µs		
L_{self}	15nH	$(dV/dt)_s$	16V/µs		
tan δ_0	$2 \cdot 10^{-4}$				
R_s	1.0mΩ				
Climatic Category 0/110/21(IEC 68-1/2)		**Design Data**			
T_{min}	- 40°C	Dimensions l × w × h	237 × 72 × 50 mm		
T_{max}	+ 110°C	Approx. weight	1.2kg		
Max. Rel. Humidity	≤ 95%	Impregnation	Resin Filled		
T_{stg}	- 45 … +110°C	Terminals	Flat Copper		
		Clearance	8 mm		
Values after Test Ca, IEC 68-2 (21 days, 40°C, 93% rel. humidity)		Creepage distance	8mm		
ΔC/C	≤ 5%	Plastic Case			
Δtanδ	≤ $4 \cdot 10^{-4}$				
R_{ins} ·C	≥ 3000s				
Mean Life Expentancy					
t_{LD}	15000h				
α_{FQ}	300fit				

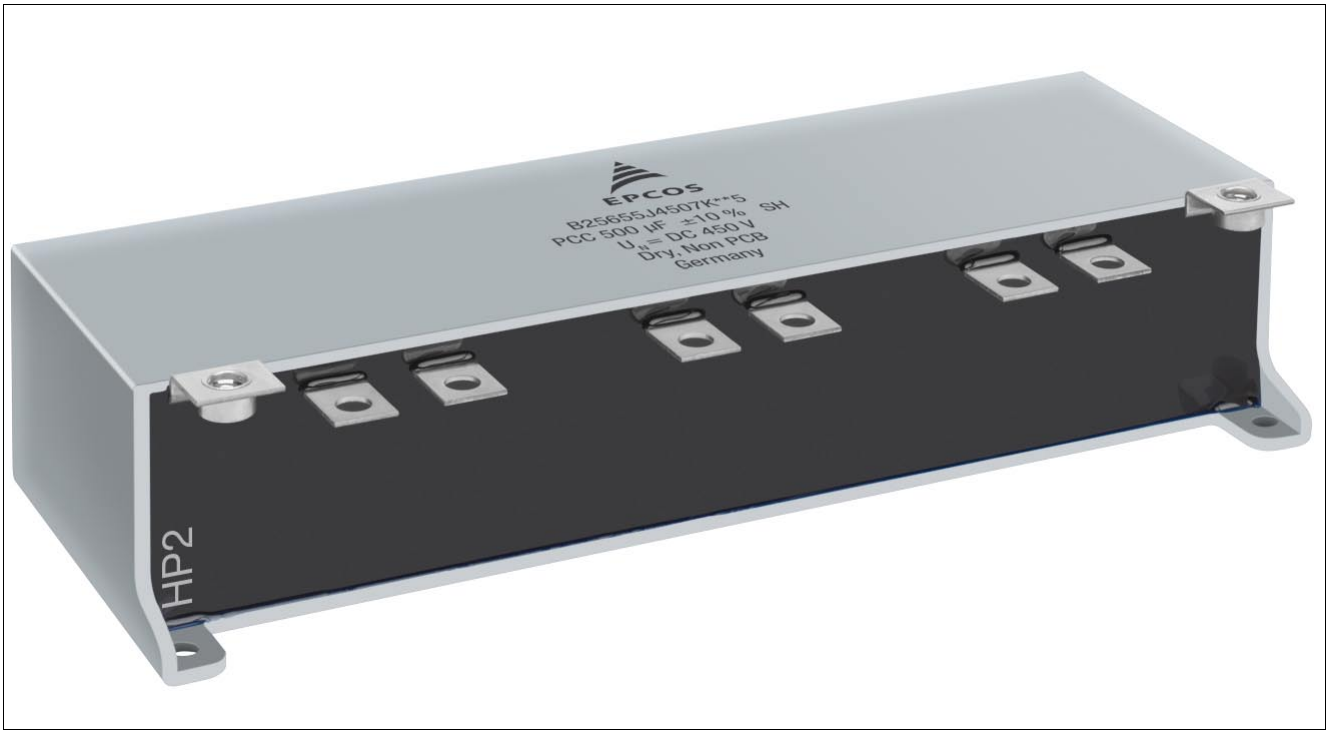


Figure 5 DC-Link Capacitor for HybridPACK™2 B25655J4507K from EPCOS AG

2.3.4.2 Kemet C4EEGMX6500AAUK

The power electronic capacitor C4EEGMX6500AAUK (see **Figure 6**) from KEMET Electronics is a metallized seal-healing polypropylene capacitor with a non-inductive winding. The plastic case is filled with resin for longterm humidity protection. Two battery connections and 6 terminals 6mm holes for the connection to the IGBTs. Electrical perfomance is given on **Figure 7**, thermal and mechanical characteristics are given in **Figure 8** and drawings are shown in **Figure 9**.

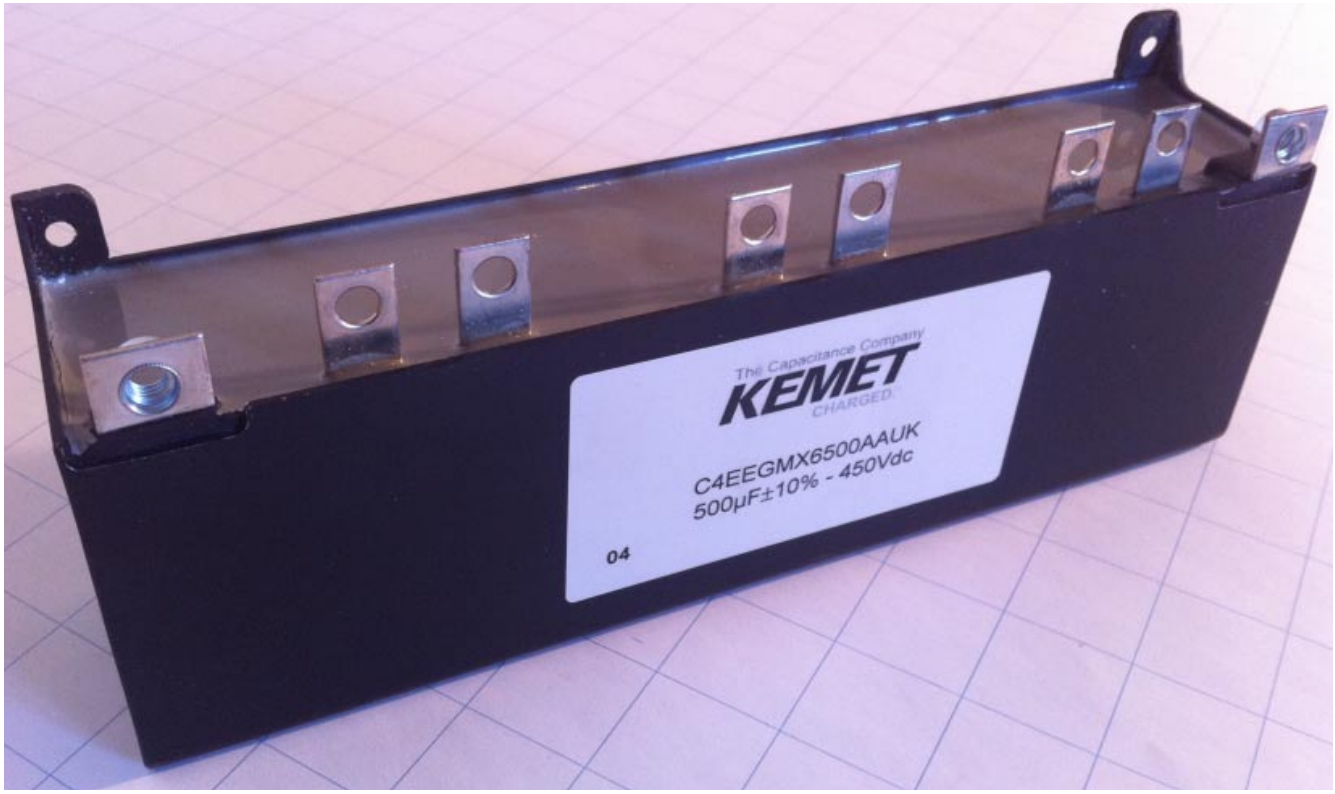


Figure 6 DC-Link Capacitor for HybridPACK™2 C4EEGMX6500AAUK from KEMET Electronics

Nominal capacitance	C_nom	500	µF	@RT ± 5°C
Tolerance	C_tol	± 10	%	
Rated DC voltage	U_rated	450	VDC	@105°C
Peak voltage	U_peak	650	VDC	for 10sec
Nominal RMS current	I_max_rms	120	A	@10kHz; T_case <105°C
Max peak current	I_peak	2500	A	@450VDC;dv/dt = 2V/µs
Equivalent Series resistance	ESR	1	mOhm	@ 1kHz
Equivalent Series inductance	ESL	15	nH	
Dissipation factor@1kHz	DF	0,01	%	@1 kHz
Max pulse rise time	(dv/dt)max	5	V/µs	
Min Insulation resistance	Ris	20	MOhm	500VDC; for120sec

Lifetime	Lexp	15000	hours	T_hotspot_max >=90°C
FIT	FIT	300	1/kpcsHours	

Figure 7 Electrical performance of C4EEGMX6500AAUK

Thermal characteristics

Operating temperature min/max	-40°C	110°C	
Storage temperature min/max	0°C	105°C	max 60% r.H
Climatic Category	40/105/56		IEC 60068-1

Mechanical characteristics

Dimensions	L x W x H	237 x 72 x 50	mm
Weight	m	1,2	Kg

Test method and performances

Voltage test between terminals @ 25°C	Ut-t	675	V/10s
Voltage test terminals to case @ 50Hz	Ut-c	2500	V/1min

Figure 8 Thermal and Mechanical Characterisics of C4EEGMX6500AAUK

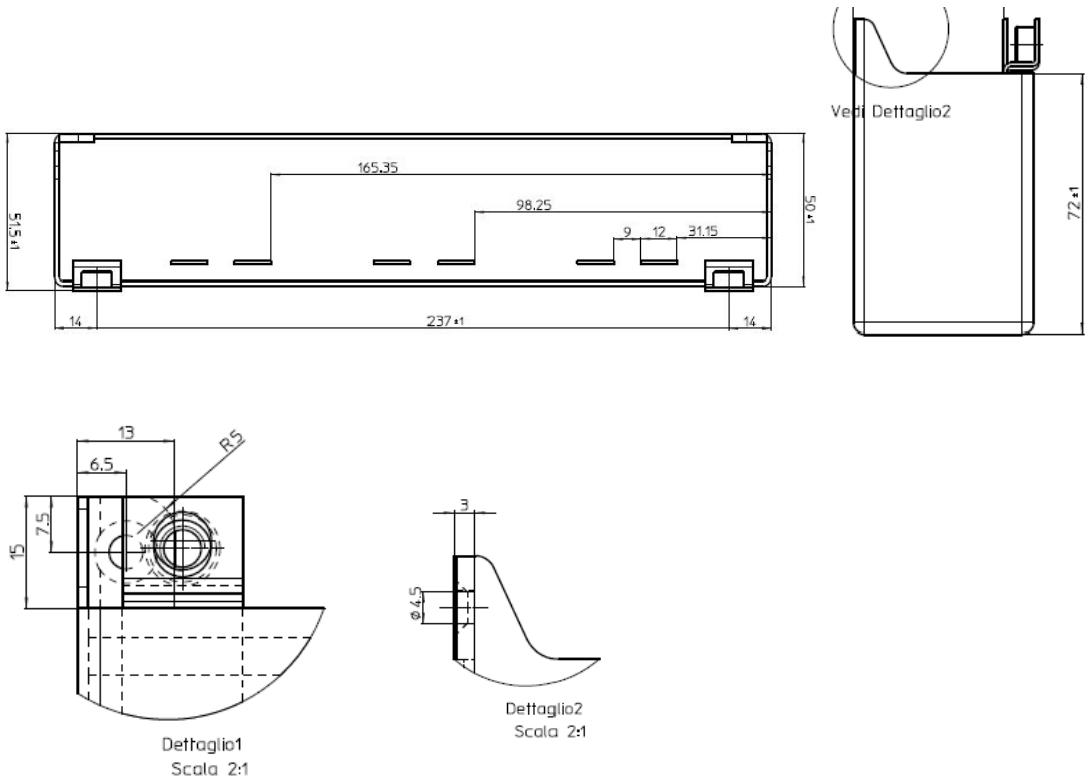


Figure 9 Drawings of C4EEGMX6500AAUK

2.3.5 Cooling Element

For applications requiring higher power or higher operation temperature a usage of water cooling element is recommended. **Figure 10** shows the low cost water cooling system that is included in the Hybrid Kit for HybridPACK™2 which can be screwed directly to HybridPACK™2 - **Figure 11** and **Figure 12** are showing the technical drawings of it.

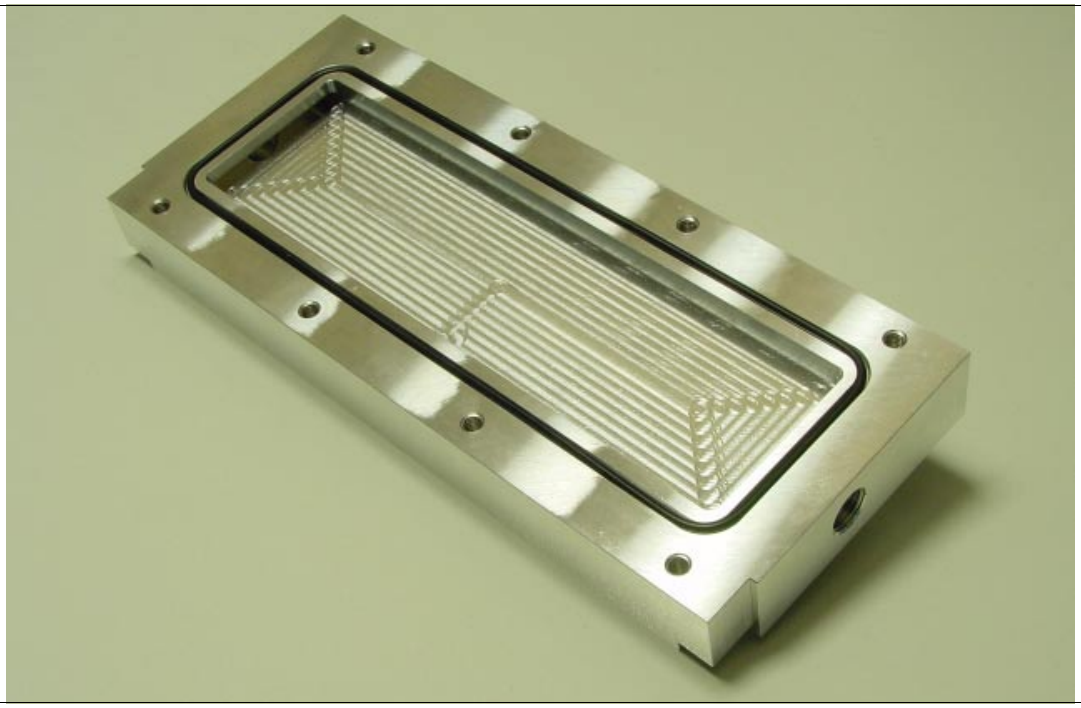


Figure 10 Example of Water Cooling Element for HybridPACK™2

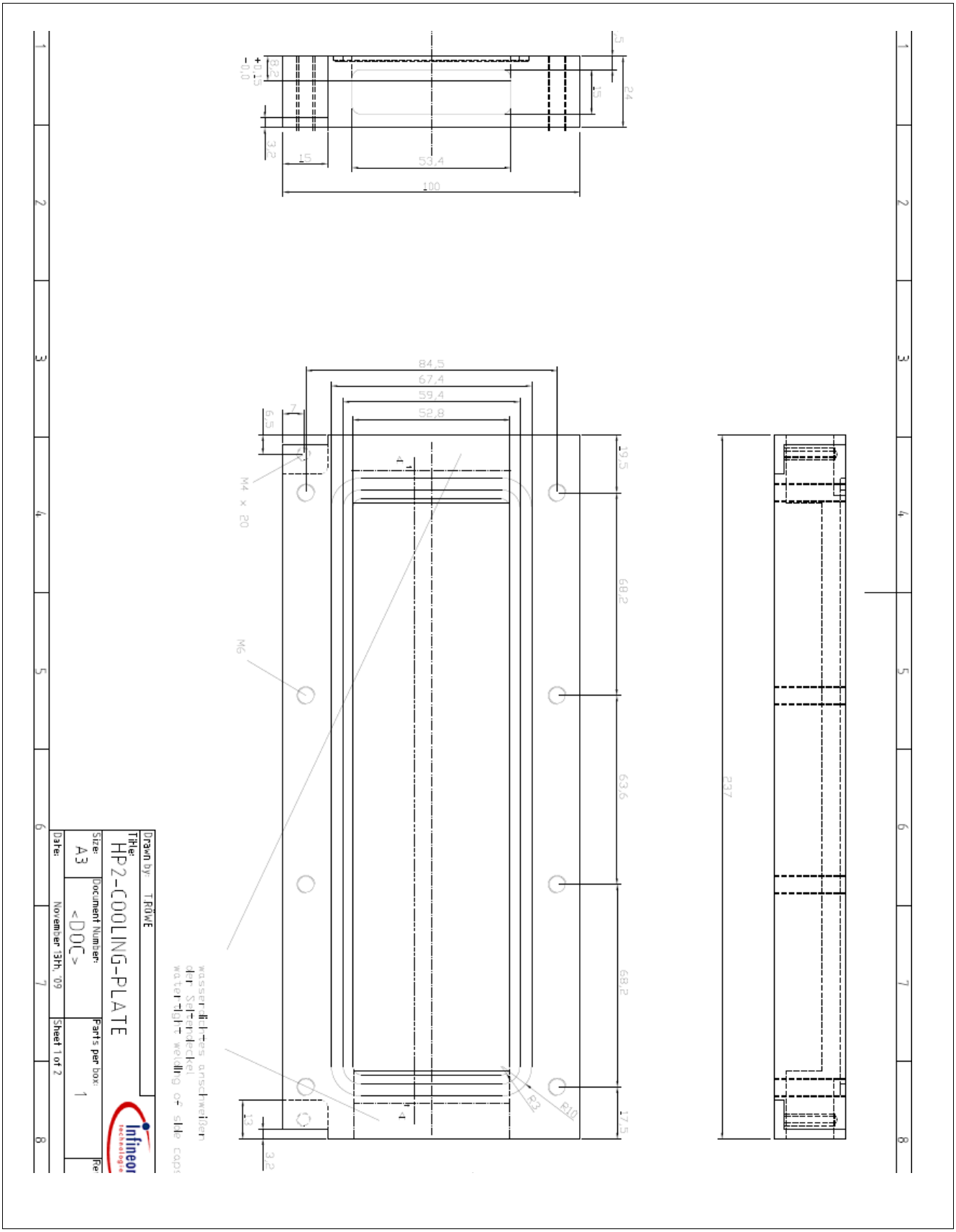


Figure 11 Water Cooling System Technical Drawings (Part 1)

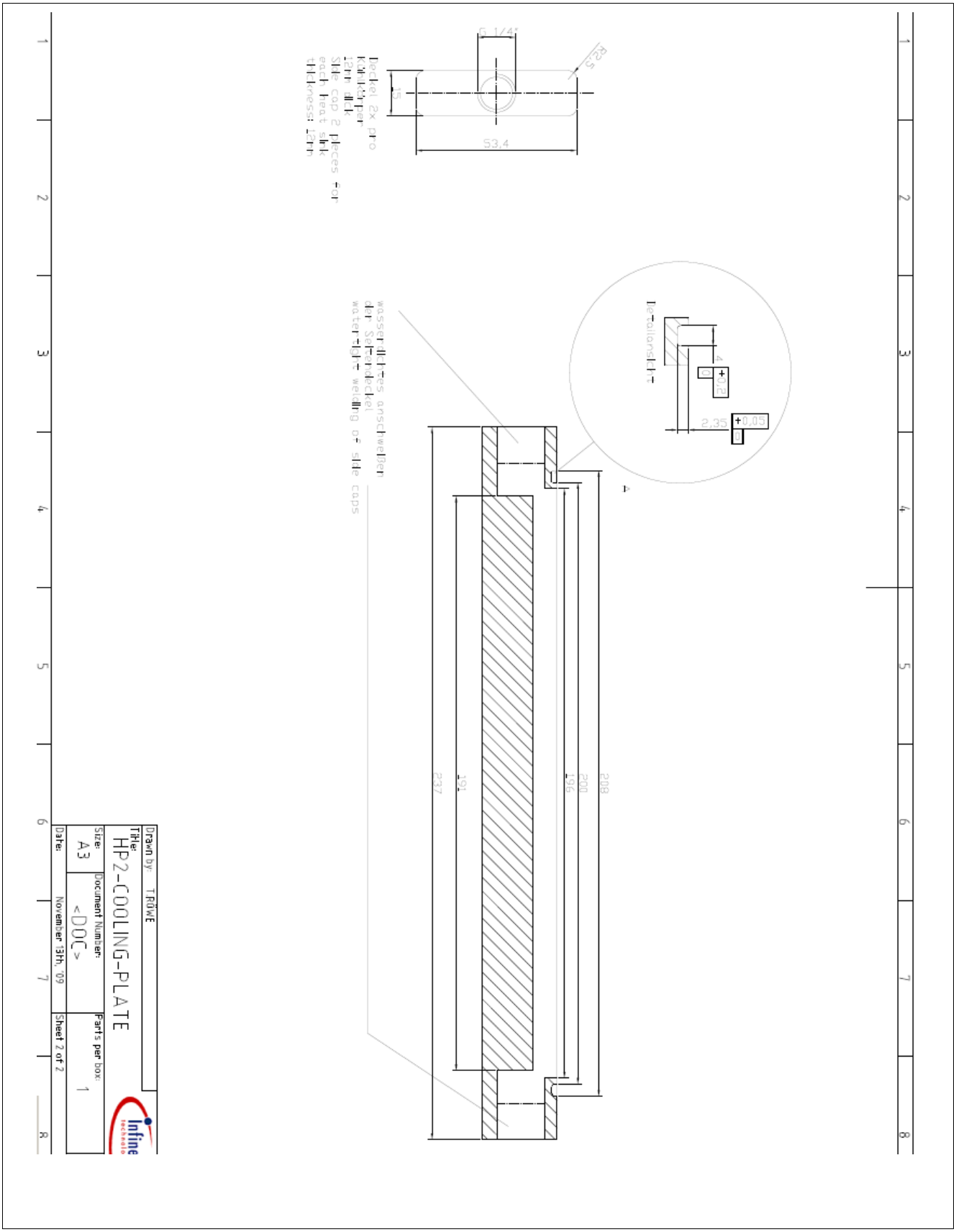


Figure 12 Water Cooling System Technical Drawings (Part 2)

3 Hybrid Kit for the HybridPACK™2 Evaluation Driver Board

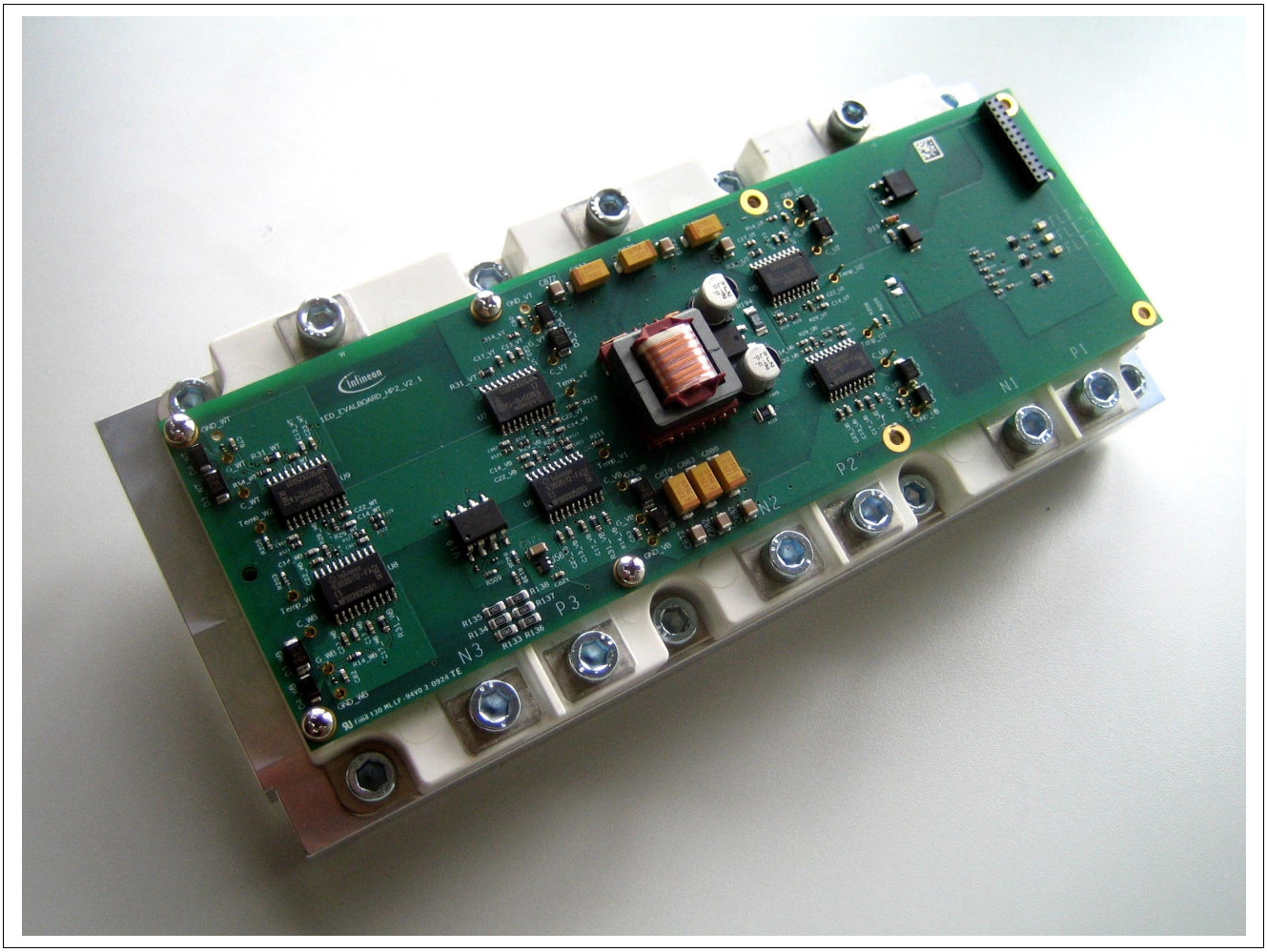


Figure 13 Driver Board Mounted on the Top of the HybridPACK™2 Module

3.1 Main Features

The Hybrid Kit for HybridPACK™2 Evaluation Driver Board offers the following features:

- Six channel IGBT driver
- Electrically and mechanically suitable for 650 V IGBT Module HybridPACK™2
- Includes DC/DC power supply
- Isolated voltage measurement
- Short circuit protection with t_{off} < 6 µs
- Undervoltage lockout of IGBT driver IC
- Positive logic with 5 V CMOS level for PWM and Fault signals
- One fault output signal for each leg and one common for all legs

Important: - if a Driver Board is used as a standalone board (without Logic Board from Hybrid Kit), the resistor R534 (please refer to **Figure 29**) should be populated (0R) to connect 2 grounds (“digital” and “analog”). If these two grounds are not connected one can notice some signal disturbances. If the Driver Board is used together with the Logic Board (as in a complete Hybrid Kit) the 2 grounds are already connected on the Logic Board (therefore it is in design of Driver Board the R534 unpopulated) and no modification (soldering) should be taken on a Driver Board.

3.2 Key Data

All values given in the **Table 2** (bellow) are typical values, measured at T_A = 25 °C

Table 2 Key Data and Characteristic Values (Typical Values)

Parameter	Value	Unit
V_{SUPPLY} – Voltage Supply	+[8...18]	V
V_{PWM} – PWM Signals for Top and Bottom IGBT (Active High)	0 / +5	V
V_{FAULT} – /FAULT Detection Output (Active Low)	0 / +5	V
I_{FAULT} – Max. /FAULT Detection Output Load Current	10	mA
V_{RST} – /RST Input (Active Low)	0 / +5	V
I_{SUPPLY} – Supply Current Consumption (Idle Mode) (V_{SUPPLY}=12V)	260	mA
V_{OUT} – Drive Voltage Level	+15 / -8	V
I_G – Maximum Peak Output Current	±10	A
$P_{DC/DC}$ – Maximum DC/DC Output Power of SMPS Unit	30	W
f_S – Maximum PWM Signal Frequency [1)]	20	kHz
t_{PDELAY} – Propagation Delay Time	200	ns
t_{PDISTO} – Input to Output Propagation Distortion	15	ns
t_{MININ} – Minimum Pulse Suppression for Turn-on and Turn-off[2)]	30	ns
V_{DESAT} – Desaturation Reference Level	9	V
d_{max} – Maximum Duty Cycle	100	%
V_{CES} – Maximum Collector – Emitter Voltage on IGBT	600	V
T_{OP} – Operating Temperature (Design Target)[3)]	-40…+125	°C
T_{STO} – Storage Temperature (Design Target)	-40…+125	°C
V_{IORM} – Maximum Repetitive Insulation Voltage [4)] (1ED020I12-FA Driver IC)	1420	V_{PEAK}
V_{ISO} – Maximum Insulation Test Voltage[5)] (1ED020I12-FA Driver IC)	4500	V_{rms}

1) The max. switching frequency for the HybridPACK™2module should be calculated separately. Limiting factors are: max. DC/DC output power of 4.6W per channel and max. PCB board temperature measured around gate resistors of 105 °C for used FR4 material. For detailed information see **Chapter 3.5.3**

2) Minimum value t_{MININ} given in 1ED020I12-FA IGBT driver datasheet

3) Maximum ambient temperature strictly depends on load and cooling conditions

4) 1ED020I12-FA datasheet - complies with DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01.Basic Insulation

5) 1ED020I12-FA datasheet - complies with UL 1577

3.3 External Connector Pin Assignment

Figure 14 shows the pin assignment for the external connector (K1) on the Driver Board. As connector is used Samtec MMS-112-01-L-DV. It includes all necessary signals to get the board into the operation, that is, supply, control and monitoring. If a Driver Board is used as a part of Hybrid Kit the communication with a Logic Board is done through this connector.

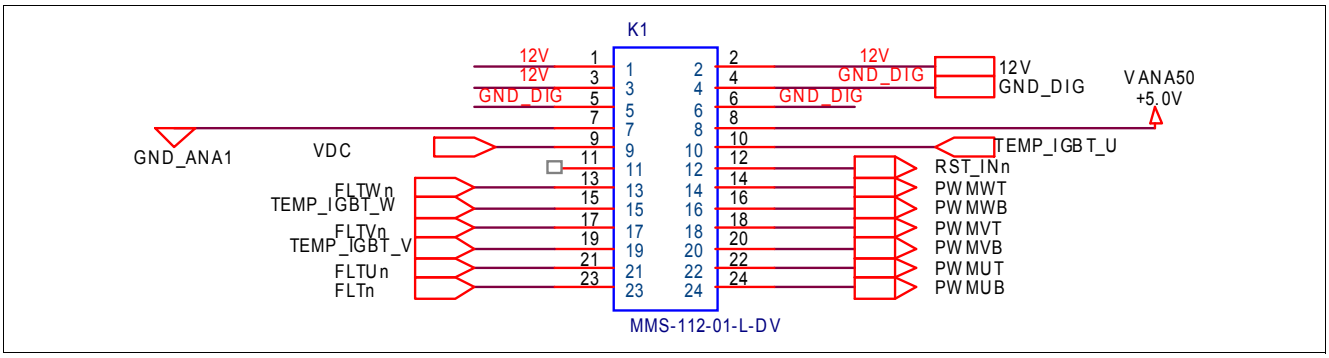


Figure 14 External Connector on the Driver Board

Pins 1 to 6 provide the power supply. The Driver Board must be supplied with an external regulated DC power supply. The input voltage must be kept between 7V and 18V (nominal 12V) and the current consumption will depend on different factors (PWM frequency, etc.). Please have on mind that if a Driver Board is used within Hybrid Kit (together with a Logic Board) the “digital” ground on K1 (pins 4, 5 and 6) is connected to the “digital” ground on the Logic Board. The same is valid for pins 1, 2 and 3 (+12V). Therefore, in the case of using of a complete Hybrid Kit, no external 12V power supply needs to be applied to Driver Board additionally - it is already done through Logic Board.

Pins 7 and 8 provide 5V analogue power supply - pin 7 supplies “analog” ground and pin 8 supplies +5V that is internally generated on Driver Board (please refer to the **Figure 29**) and intended to be used as a power supply for the temperature and DC bus voltage measurements. Although available on the pin 8 of connector K1, the +5V analogue power supply is not connected to the +5V analogue supply of the Logic Board - on the other side, through pin 7 on K1 the “analog” grounds on Driver and Logic Board are mutually connected.

To pins 9, 10, 15 and 19 are connected monitoring signals: DC-link voltage measurement and temperature measurement of the three different phases inside of the IGBT module.

Pins 14 (phase W, top IGBT), 16 (phase W, bottom IGBT), 18 (phase V, top IGBT), 20 (phase V, bottom IGBT), 22 (phase U, top IGBT) and 24 (phase U bottom IGBT) contain the logic signals for controlling the 6 drivers on the Driver Board. These PWM signals are generated by TriCore TC1767 on the Logic Board in the case that a Driver Board is used as a part of a Hybrid Kit - if a Driver Board is not used as a part of Hybrid Kit the PWM signals should be supplied through these pins.

Pins 12 is a Reset signal (to control the IGBT drivers 1ED020I12-FA).

Pins 13, 17, 21 and 23 contain Fault Detection signals - one for each phase and one as logical “AND” combination of 3 phase fault Detection signals.

3.4 Mechanical Dimensions of the Driver Board

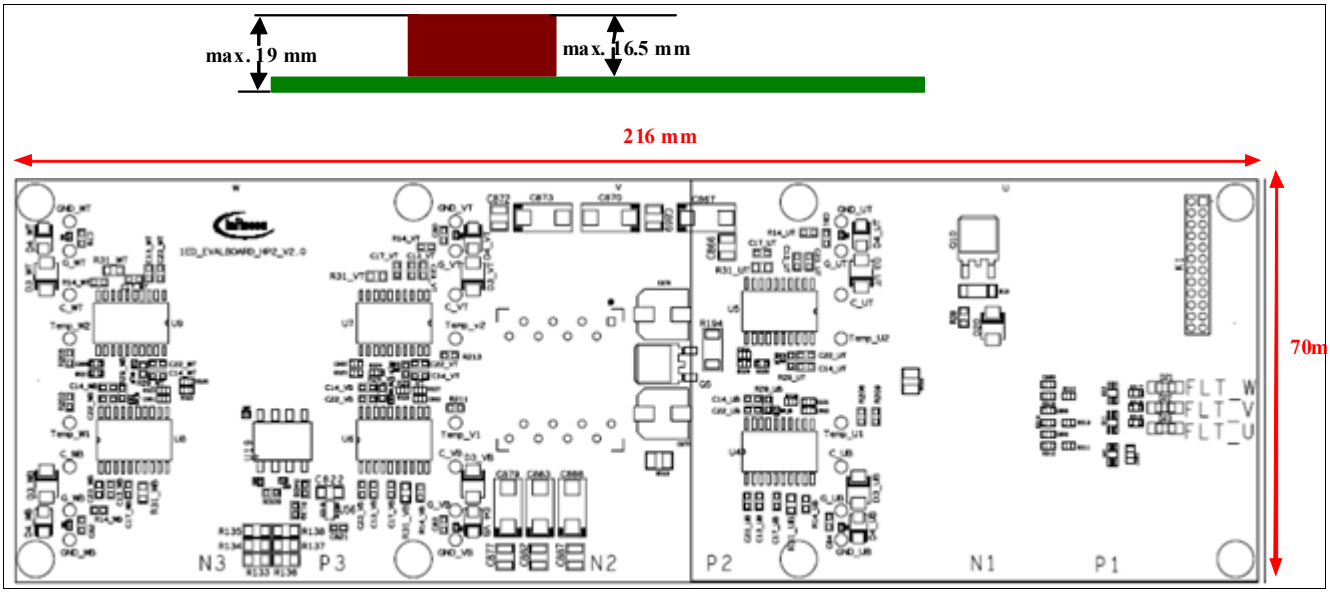


Figure 15 Dimensions of the Driver Board

The Driver Boards should be fastened by self taping screws and soldered to the auxiliary connectors on top of the IGBT module. The contact joints (solder points) between PCB and module auxiliary contacts should be mechanically relieved in order to disburden the solder connection as far as possible. Relieve of the contact points is carried out by mounting the PCB directly onto the module at the ten mounting stand-offs (see **Figure 16**) using self-tapping screws (thread forming with 2.5mm diameter) or similar assembly material. The screws should be mounted in the sequence showed in **Figure 16**.

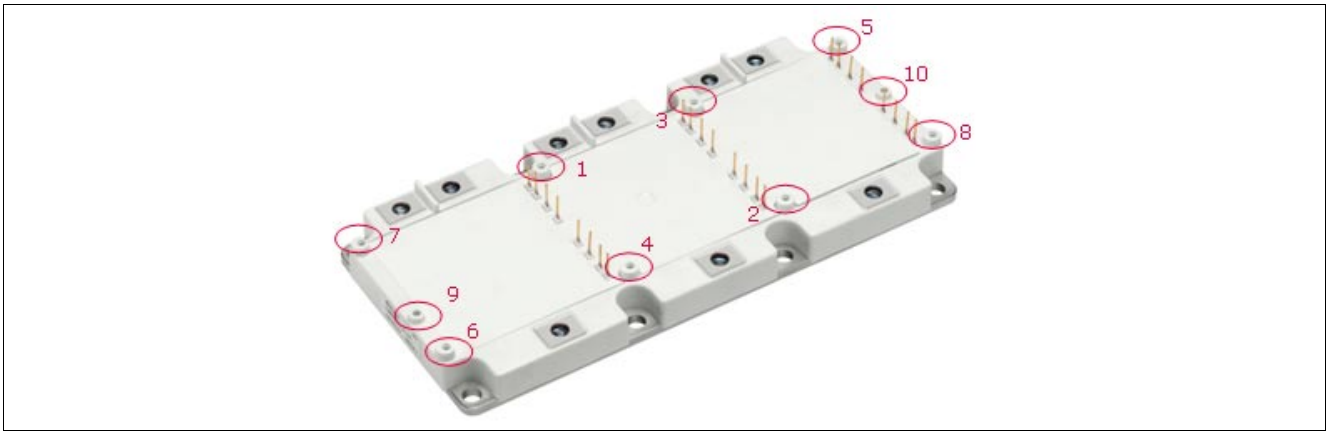


Figure 16 PCB Mounting Stand-offs of HybridPACK™2

3.5 Operation of the Driver Board

Figure 17 shows the block structure of the Driver Board. The following chapter describes these blocks in detail.

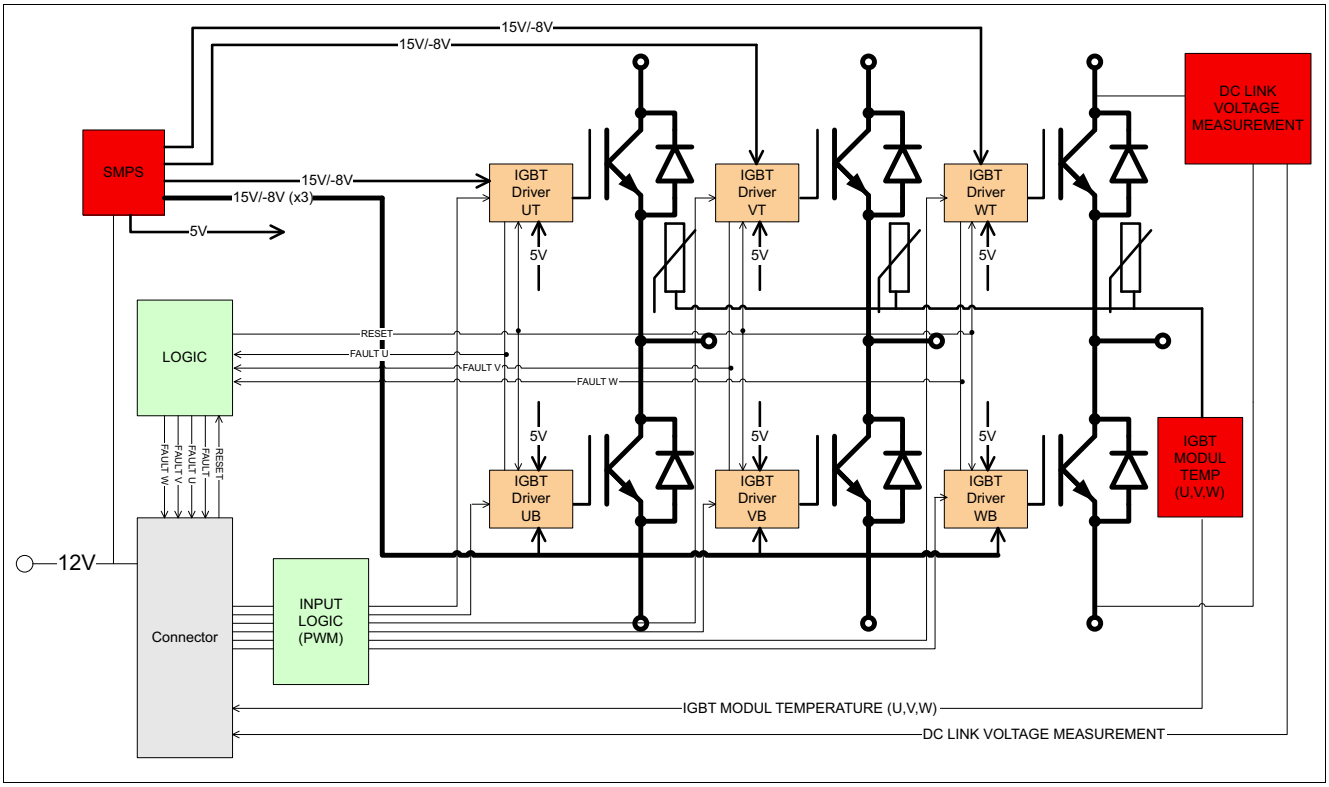


Figure 17 Hybrid Kit for the HybridPACK™2 Evaluation Driver Board Block Diagram

3.5.1 Switching Mode Power Supply (SMPS)

The Driver Board has an integrated DC/DC converter which generates the required secondary isolated unsymmetrical supply voltage of +15/-8V. Top and bottom driver voltages are independently generated by using one unipolar input voltage of 12V.

An additional supply voltage (5V) is generated and forwarded to the external connector (K1, pin 7 and 8), so if a Driver Board is used as a standalone board, it can be used to supply external components in the system (current measurement, motor interface, etc.)

For circuit details please refer to **Figure 29**.

3.5.2 Input Logic

The Driver Board is a dedicated system for a six-pack HybridPACK™2 IGBT configuration - therefore it is necessary to use 6 separated PWM signals. The schematics on **Figure 18** shows the input logic block with +5V positive logic. The block is made up of RC filters for each PWM signal in order to reduce noise. Additionally these signals are pulled-down in order to avoid unwanted switching-on of the drivers. Please have on mind that the Hybrid Kit for HybridPack™2 does not provide dead time automatically (meaning that hardware alone provides no dead time) - it is up to the user to generate the PWM signals with the correct dead time (by means of software).

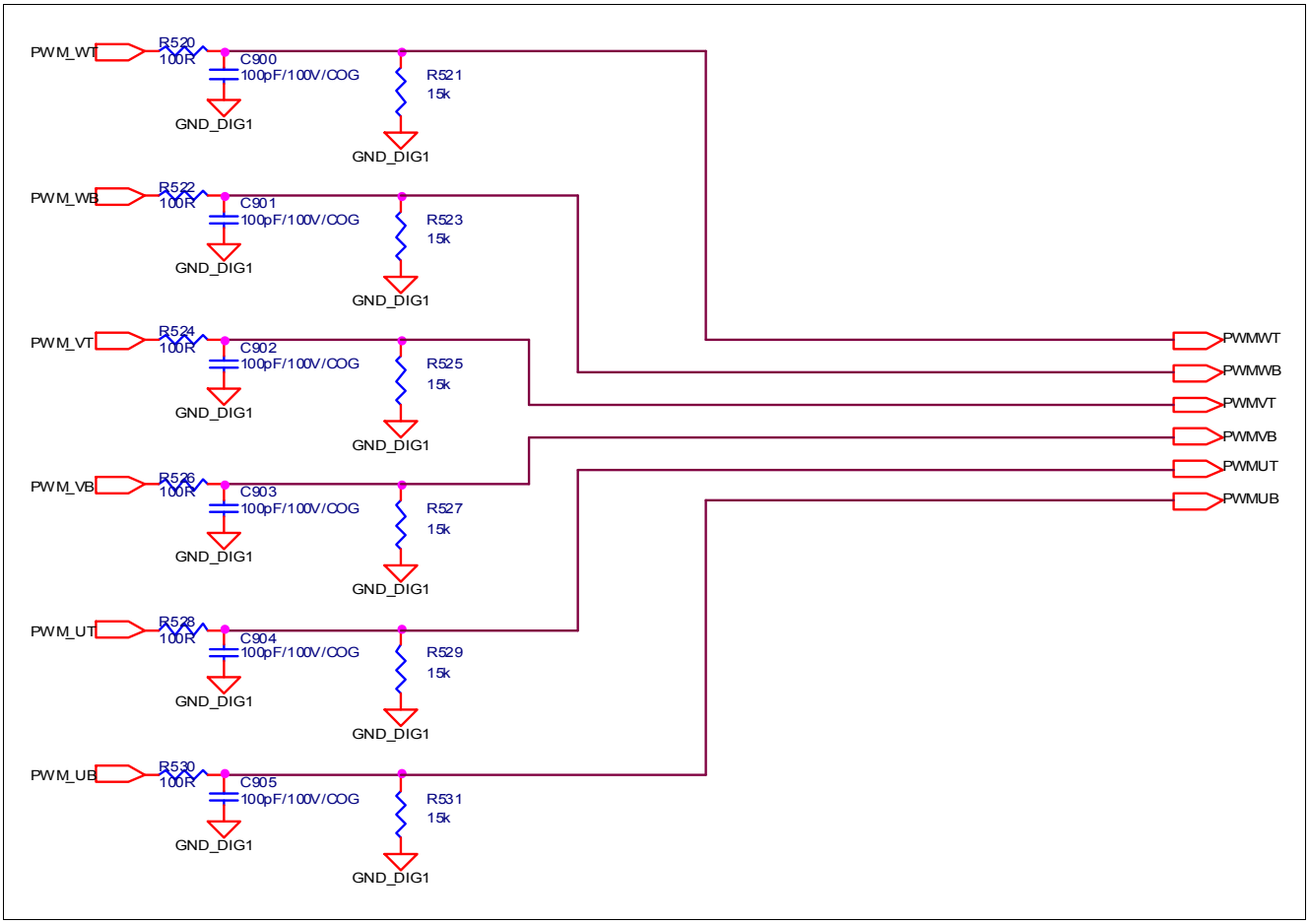


Figure 18 Schematic of the Input Logic Block of the Driver Board

3.5.3 IGBT Switch-off Behavior

Due to the stray inductances of the system a voltage overshoots occur during the switching-off the IGBT. Such overshoots are added to the DC-link voltage, so that the maximum blocking voltage of the IGBT or capacitor might be exceeded causing damages in both components (DC link capacitor and IGBT module). In order to avoid such risks an active clamping circuit is used (see **Chapter 3.5.6**).

Without such protection methods the maximum current would be limited by the DC-link voltage and the voltage overshoots at switching-off. The voltage overshoots can be minimized by increasing the gate resistor, which will reduce the di/dt value. **Figure 19** shows the maximal switch-off current at different DC-link voltages for a different values of the gate resistor. These results were obtained with the DC-link capacitor described in **Chapter 2.3.4**.

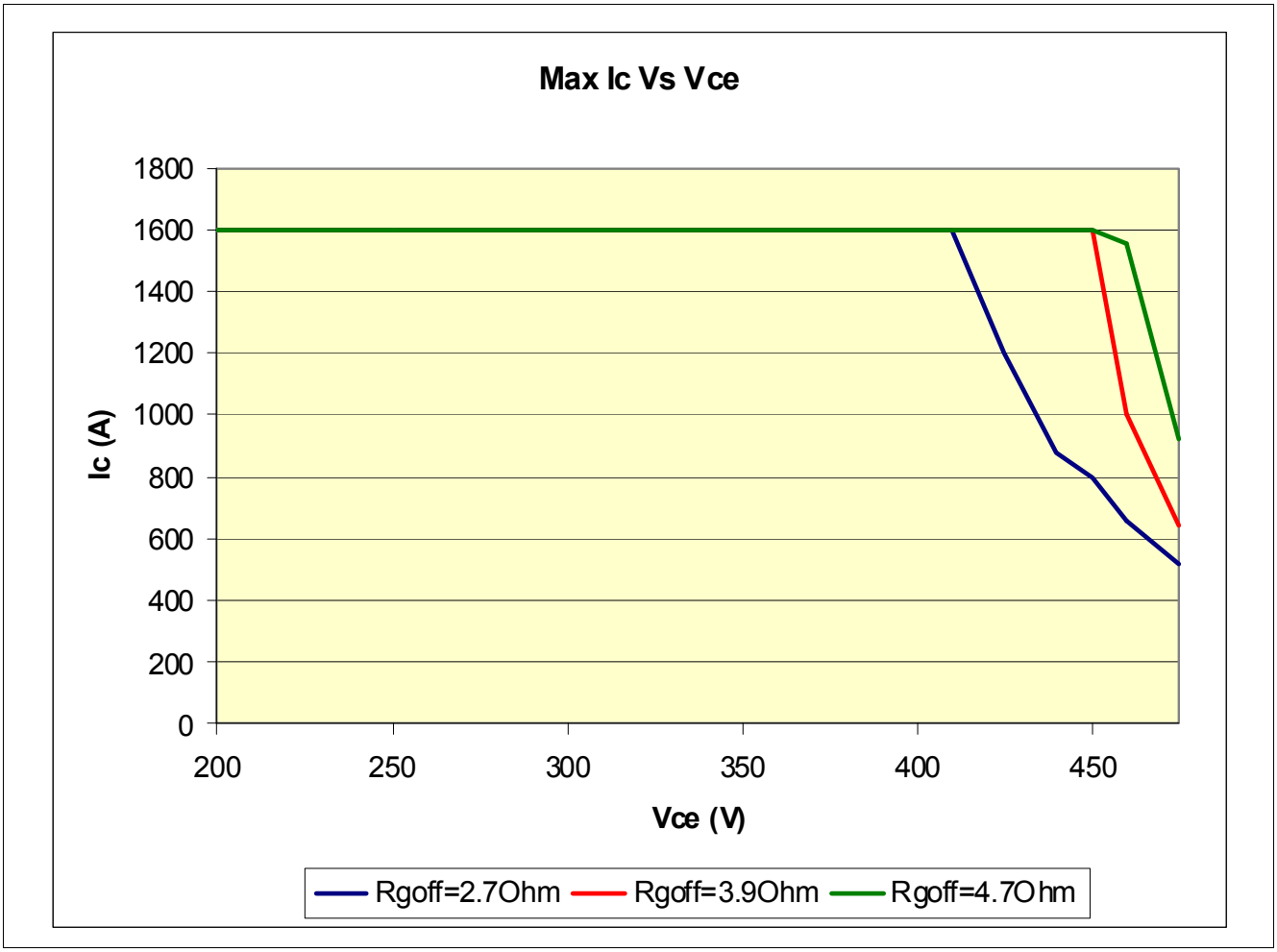


Figure 19 Maximal Switch-off Current at Different DC-Link Voltages (Gate Resistance as a Parameter)

3.5.4 Maximum Switching Frequency

The IGBT switching frequency is limited by the available power and by PCB temperature. According to theory the power losses generated in the gate resistors are a function of a gate charge, voltage step at the driver output and switching frequency. The energy is dissipated mainly through the PCB and raises the temperature around the gate resistors. When the available power of the DC/DC converter is not exceeded, the limiting factor for the switching frequency is the absolute maximum temperature for the FR4 material. The allowed operation temperature is 105 °C.

Generally the power losses generated in the gate resistors can be calculated according to **Equation (1)**:

$$P_{dis} = P_{R_{Gext}} + P_{R_{Gint}} = \Delta V_{out} \cdot f_S \cdot Q_{ge} \quad (1)$$

In **Equation (1)** f_S resembles the switching frequency, ΔV_{out} represents the voltage step at the driver output, P_{dis} is the dissipated power, Q_{ge} is the IGBT gate charge value corresponding to +15V/-8V switching operation. This value can be approximately calculated from the datasheet value by multiplying it by 0.77, that is $Q_{ge} = 6.6\mu C$. Therefore the maximum frequency limited by the available power will be:

$$f_{Smax} = 4.6W/(23V \cdot 6.6\mu C) = 30.3kHz$$

Figure 20 shows experimentally determined board temperature dependencies with switching frequency (at 26°C ambient temperature). From **Figure 20** it can be concluded that the maximum switching frequency is limited by PCB temperature.

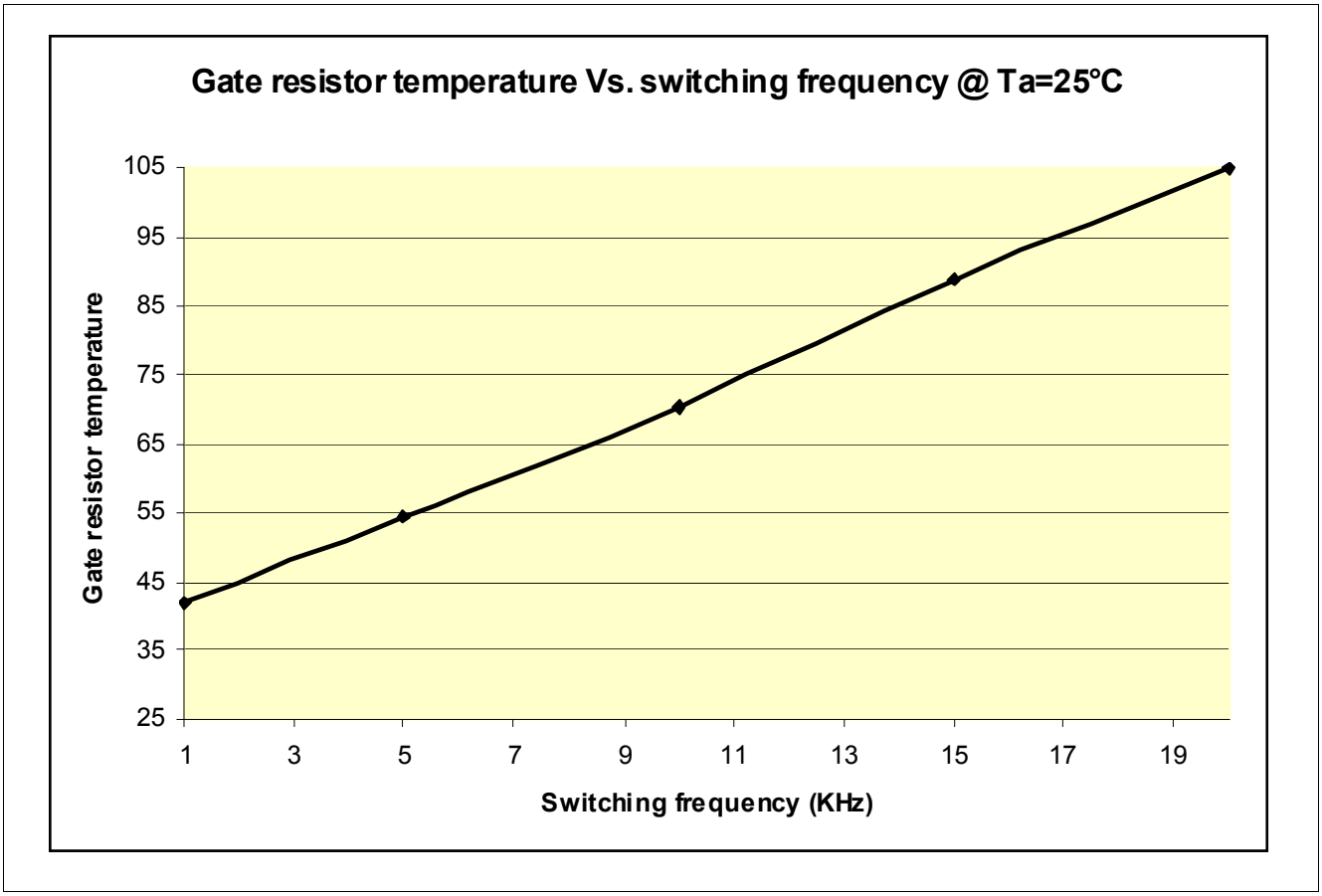


Figure 20 Temperature of Gate Resistors vs. Switching Frequency

3.5.5 Booster

Two transistors per driver IC are used to amplify the driver ICs signals. On this way the driving IGBTs are supplied with sufficient current even if driver ICs alone can't deliver enough current. One NPN transistor is used for switching the IGBT on and another PNP transistor for switching the IGBT off.

The transistors are dimensioned to have enough peak current to drive HybridPACK™2 modules. Peak current can be calculated like in **Equation (2)**:

$$I_{peak} = \frac{\Delta V_{out}}{R_{G_{int}} + R_{G_{ext}} + R_{Driver}} \quad (2)$$

For circuit details please refer to **Figure 33**.

3.5.6 Short Circuit Protection and Clamp Function

The short circuit protection of the Driver Board basically relies on the detection of a voltage level higher as 9 V on the DESAT pin of the 1ED020I12-FA driver IC and the implemented active clamp function. Thanks to this operation mode, the collector-emitter overvoltage, which is a result of the stray inductance and the collector current slope, is limited. Depending on the stray inductance, the current and the DC voltage the voltage overshoot during turn off changes. **Figure 21** shows the parts of the circuit needed for the desaturation function and the active clamping function.

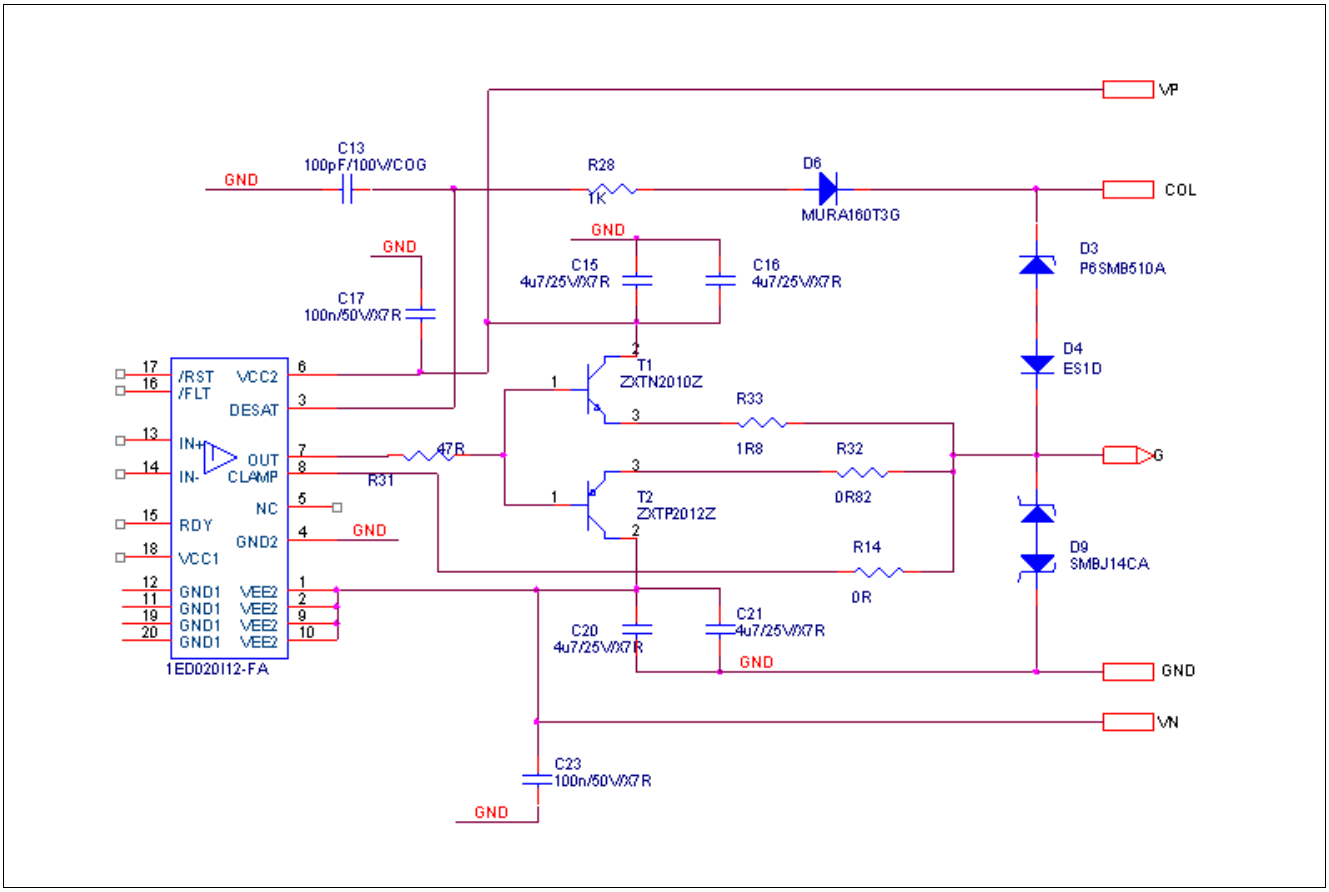


Figure 21 Desaturation Protection and Active Clamping Diodes

In the case of a short circuit the collector-emitter saturation voltage will rise and the driver detects the short circuit occurrence - to protect the IGBT it has to be turned off. As a consequence of IGBT turn-off process there will occur an voltage overshoot due to the stray inductance of the module and the DC-link. This voltage overshoot has to be lower than the maximum IGBT blocking voltage. Therefore the Driver Board has an active clamping function whereby the clamping will increase the voltage for the booster and also increase the voltage directly on the gate.

The typical turn-off waveform under short circuit condition and room temperature of a HybridPACK™2 module without any additional protective functions is shown in **Figure 22** a). Typical waveform under short circuit condition with active clamp function at room temperature is shown in **Figure 22** b). As it can be seen, the voltage overshoot without active clamping at a DC voltage of 275V is close to the maximum IGBT blocking voltage of HybridPACK™2 (650V), which could damage the devices. With active clamping the voltage overshoot can be reduced and the DC voltage increased without damaging the IGBT module (at 400V DC voltage can be observed voltage overshoot of approximately 604V, **Figure 22** b). In design are implemented 510V clamping diodes. The level of the clamping voltage must be adjusted depending on the application.

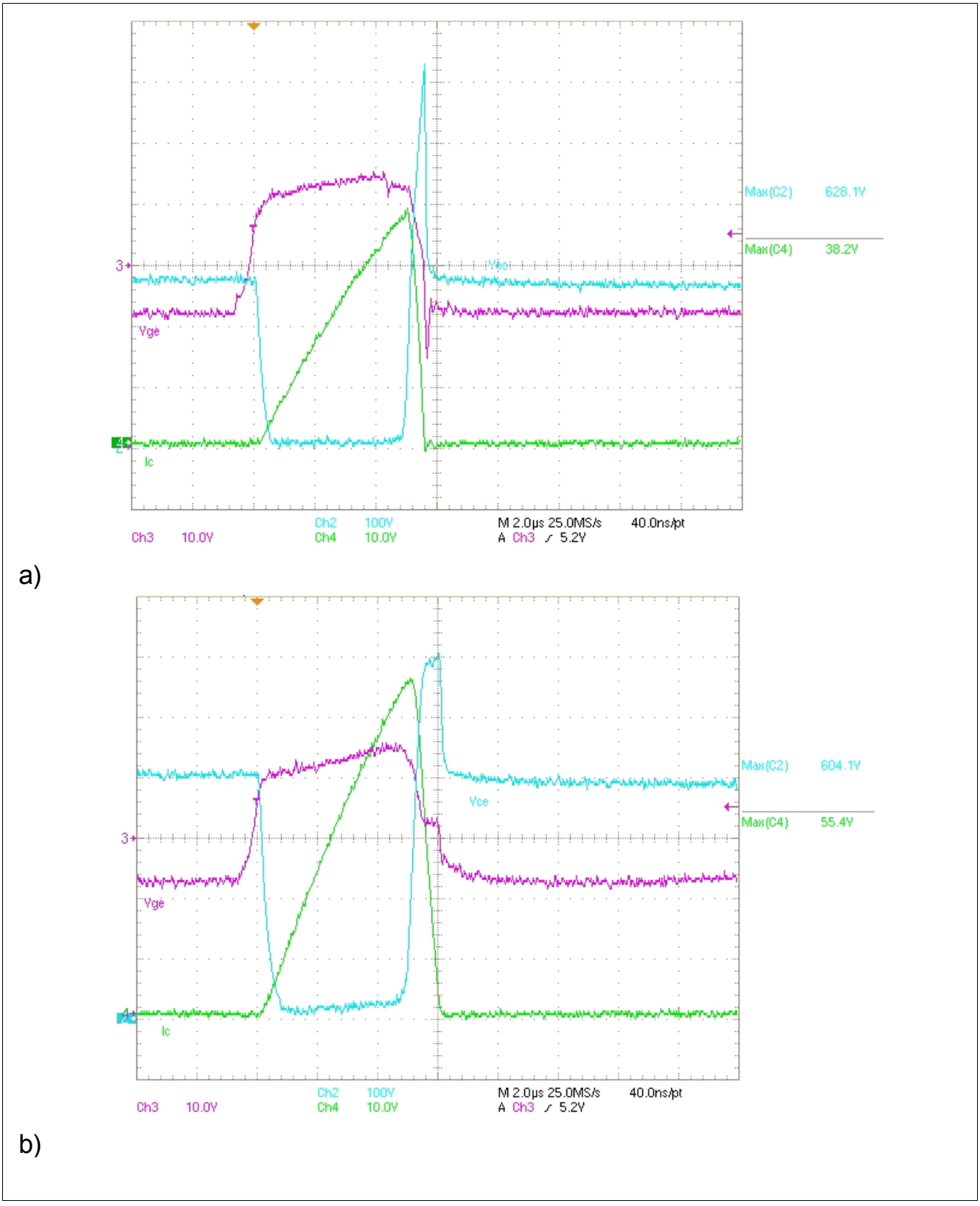


Figure 22 a) Short Circuit w/o Active Clamp (DC Voltage=275V, Voltage Overshoot=628V)
b) With Active Clamp Function (DC Voltage=400V, Voltage Overshoot=604V)

3.5.7 Fault Output

When a short circuit occurs the voltage V_{CE} is detected by the desaturation protection of the 1ED020I12-FA and the IGBT is switched off. The fault is reported to the primary side of the driver as long as there is no reset signal applied to the driver. The fault signal (/FLT) is active low - the schematic of design implemented in Driver Board can be seen on **Figure 23**.

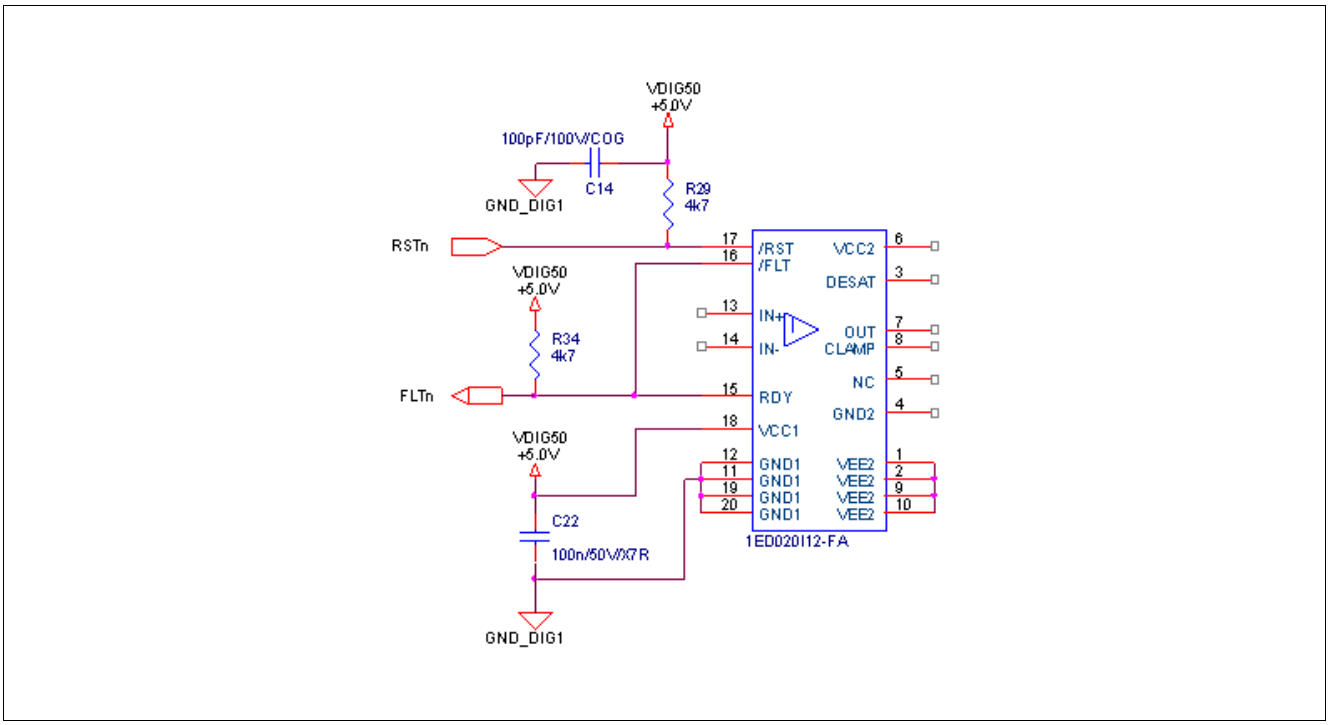


Figure 23 Fault Output of a Single Driver IC

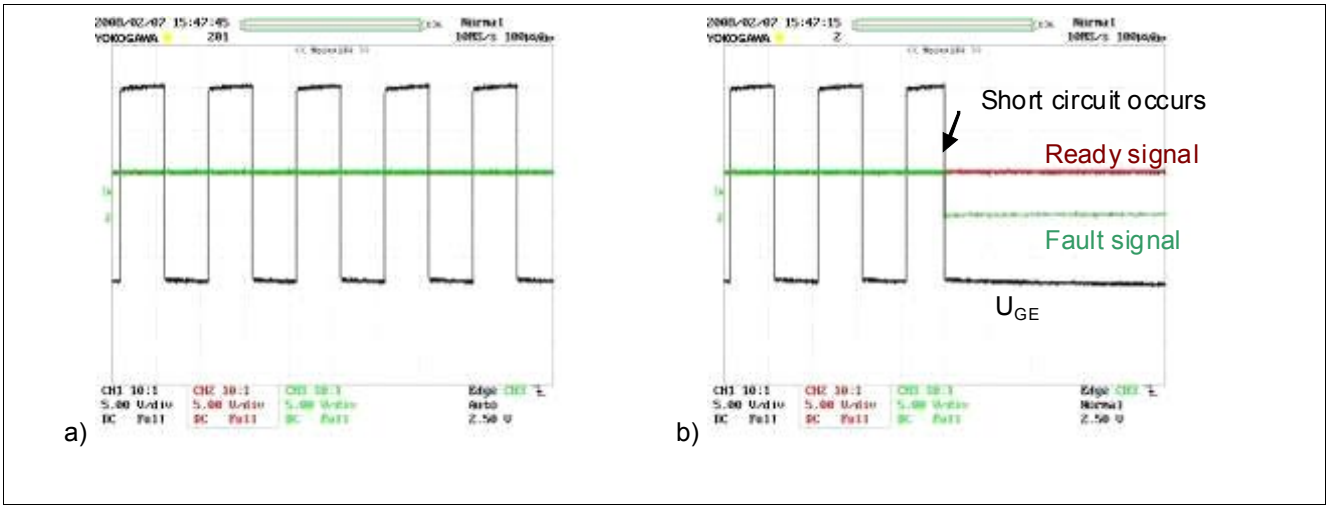


Figure 24 Fault Output During: a) Normal Operation b) Operation under Short Circuit

The fault signal (/FLT) will be in low state if a short circuit occurs and will remain low until /RST signal is pulled down.

On the Driver Board each of the three legs has its own fault signal (FAULTUn, FAULTVn, FAULTWn). As it can be seen in **Figure 31**, a LED will warn in the case of a DESAT-FAULT condition in one of the phases. The three fault signals are connected to a logical AND gate and the output of this gate, together with the 3 phases fault signals, is forwarded to the external connector (K1).

3.5.8 Temperature Measurement

The IGBT module HybridPACK™2 includes three integrated NTC (Negative Temperature Coefficient) sensors which simplify the thermal measurements in inverters significantly.

The NTCs are located on the same ceramic substrate together with the IGBT and diode chips. The module is filled with silicon gel for isolation purpose and under normal operation conditions the requirements for isolation voltages are met. The NTC isolation capability is tested with 2.5kV AC in final test for 1 minute for 100% of module production.

The NTCs are connected to the main connector K1 (pins 10, 15 and 19) by means of the circuit showed in **Figure 36**. **Figure 25** shows the relationship between IGBT module base plate temperature of the three phases and output voltage of IGBT module temperature block (TEMP_IGBT_U, TEMP_IGBT_V, TEMP_IGBT_W, K3.10/K3.19/K3.15)

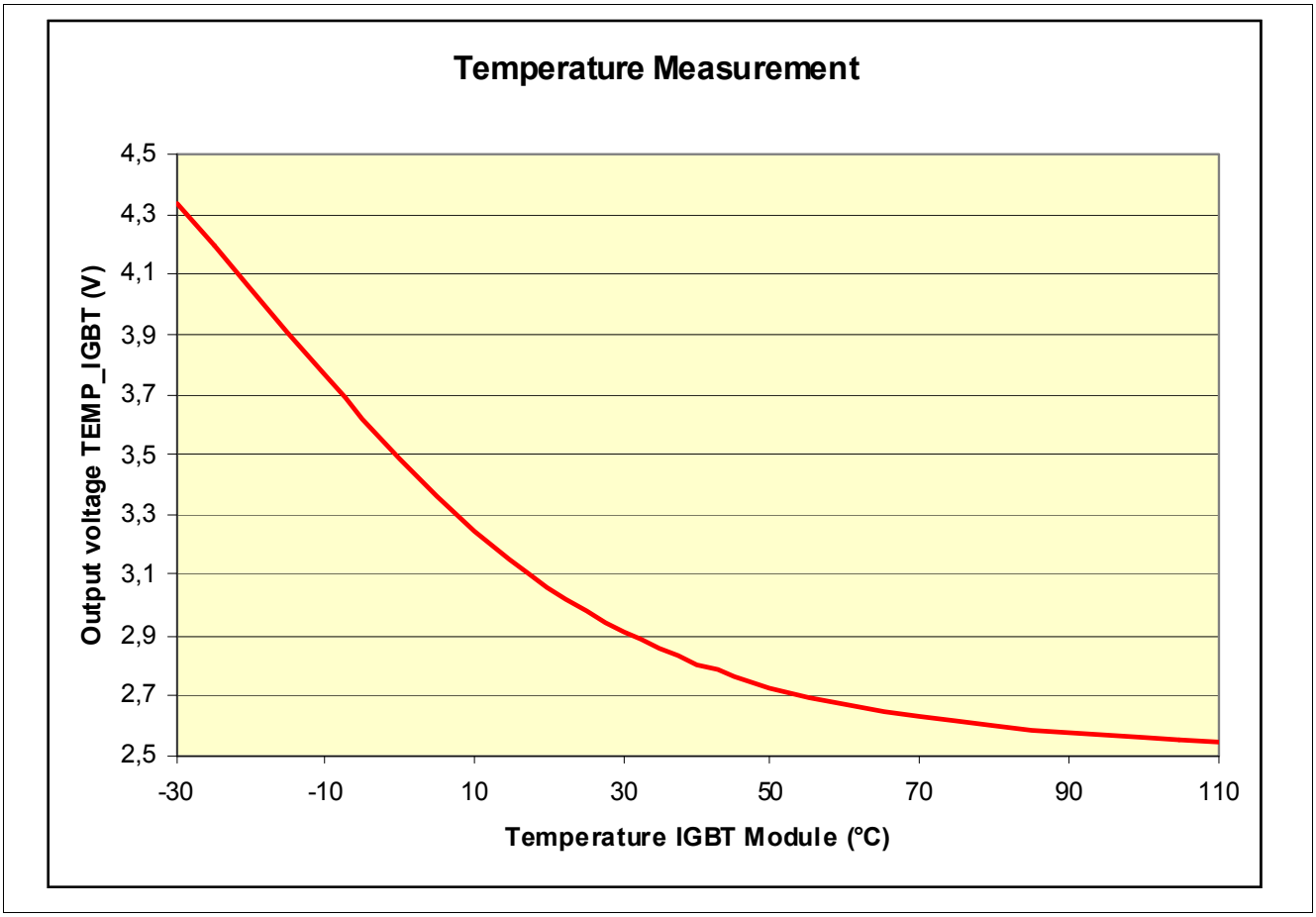


Figure 25 Characteristics of the Temperature Measurements

Note: This temperature measurement is not suitable for the short circuit or short term overload detection and should be used only for the module protection against long term overload or malfunction of the cooling system.

3.5.9 DC Voltage Measurement

On the Hybrid Kit for HybridPACK™2 the voltage at the DC link is measured by means of a isolation amplifier which offers the necessary galvanic isolation (see **Figure 35**).

The output of this circuit is connected to the external connector (Vdc, K1.9). **Figure 26** shows the relationship between DC link voltage and Vdc output signal.

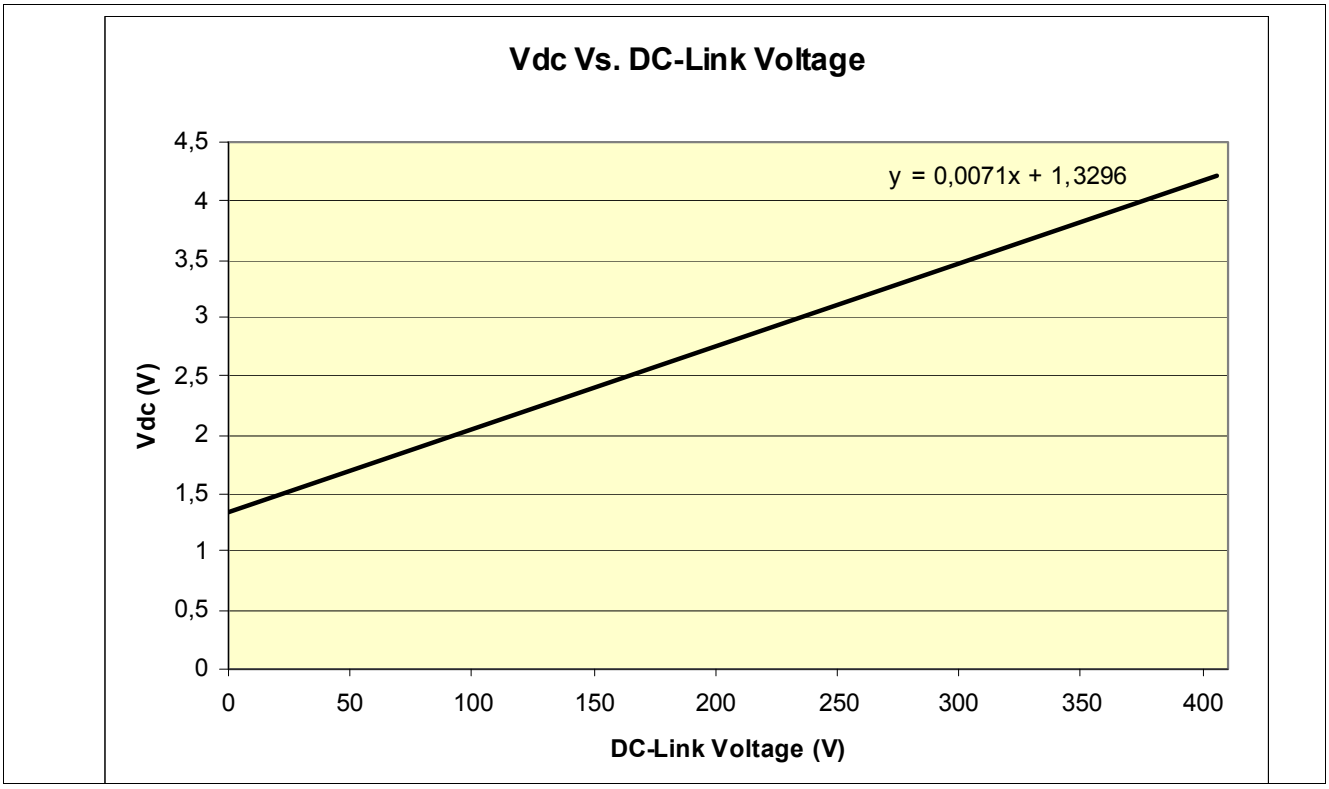


Figure 26 Characteristics of the DC Voltage Measurement

3.6 Switching Losses

Switching losses can be different comparing to the values given in the HybridPACK™2 IGBT module datasheet. Main reason for this discrepancy is that switching voltages used on the Driver Board (+15V for turn-on and -8V for turn-off) differ from HybridPACK™2 characterisation switching voltages (+15V/-15V).

Turn-on losses are expected to be close to the values of the datasheet of HybridPACK™2, but as mentioned, this will be different for the turn-off losses. In general the turn-off losses depend on the stray inductances of the DC-link and increase linear with the DC-link voltage. In the case of the Driver Board the turn-off losses do not increase linearly because of the fact that the active clamping feature increases the turn-off losses due to decrease of the di/dt.

3.7 Definition of Layers of Driver Board

The Driver Board was made keeping the following rules for the copper thickness and the space between different layers shown in **Figure 27**.

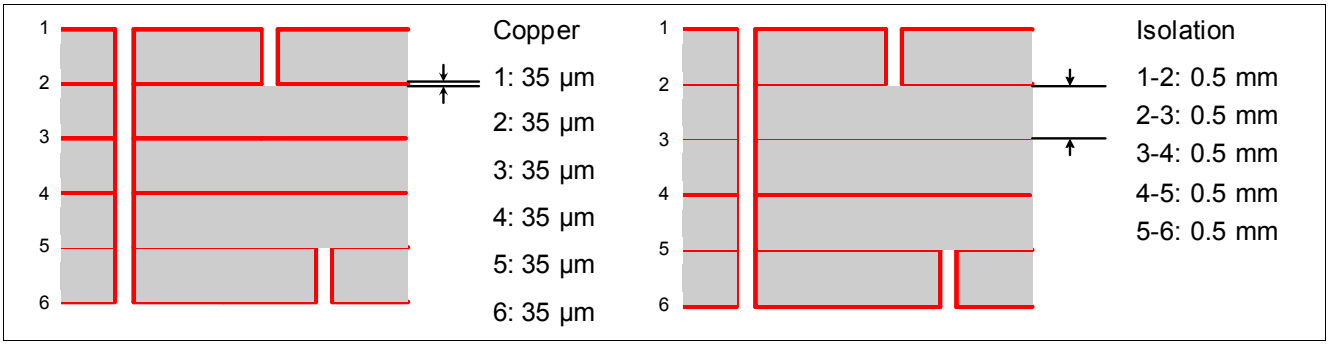


Figure 27 Copper and Isolation for Layers of Driver Board

3.8 Schematics, Layout and Bill of Material

To meet the individual customer requirements and to make the Driver Board for the HybridPACK™2 module as a platform for development or modifications, all necessary technical data like schematics, layout and components are included in this chapter.

3.8.1 Schematics

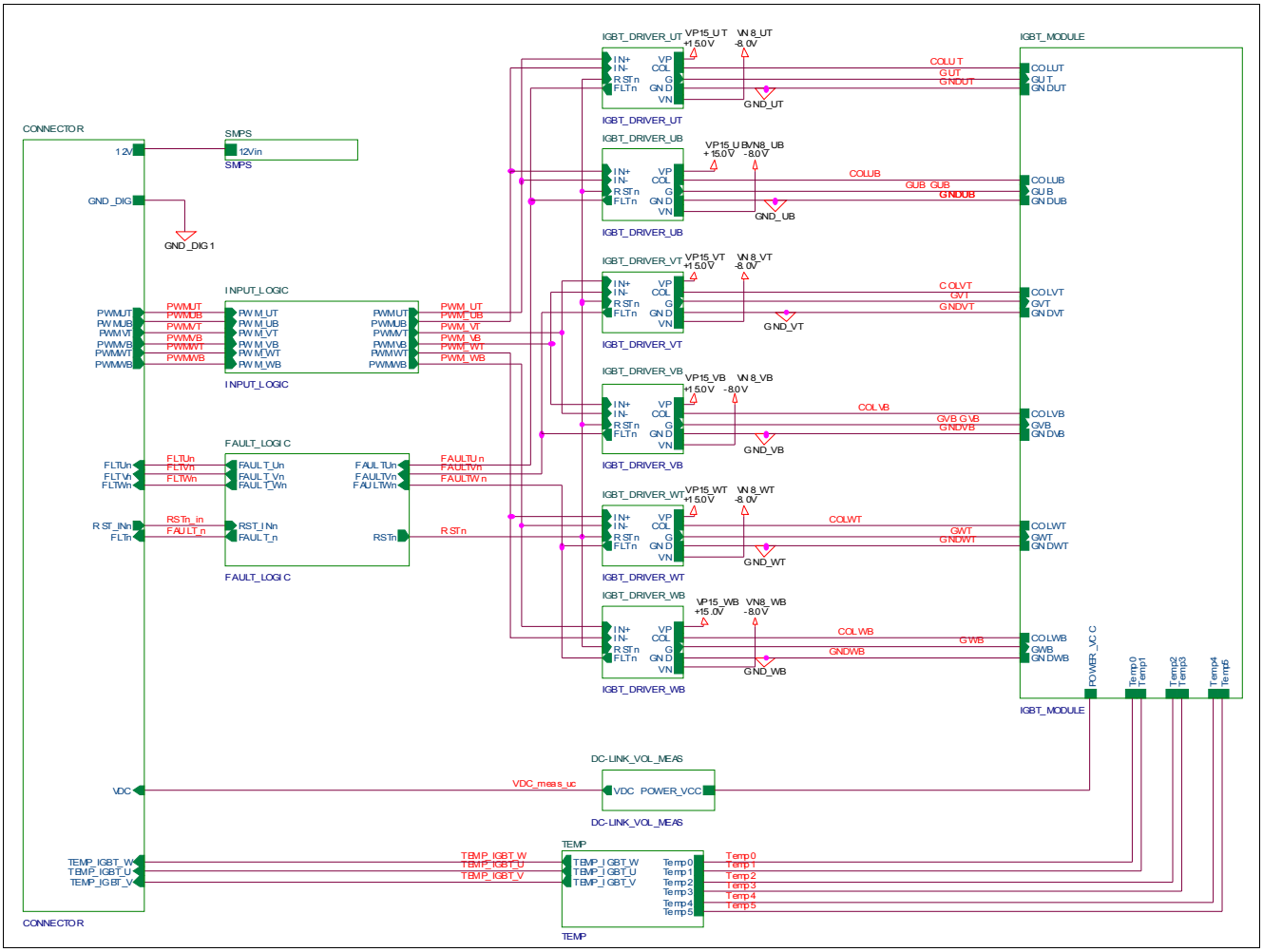


Figure 28 Schematics Block Overview

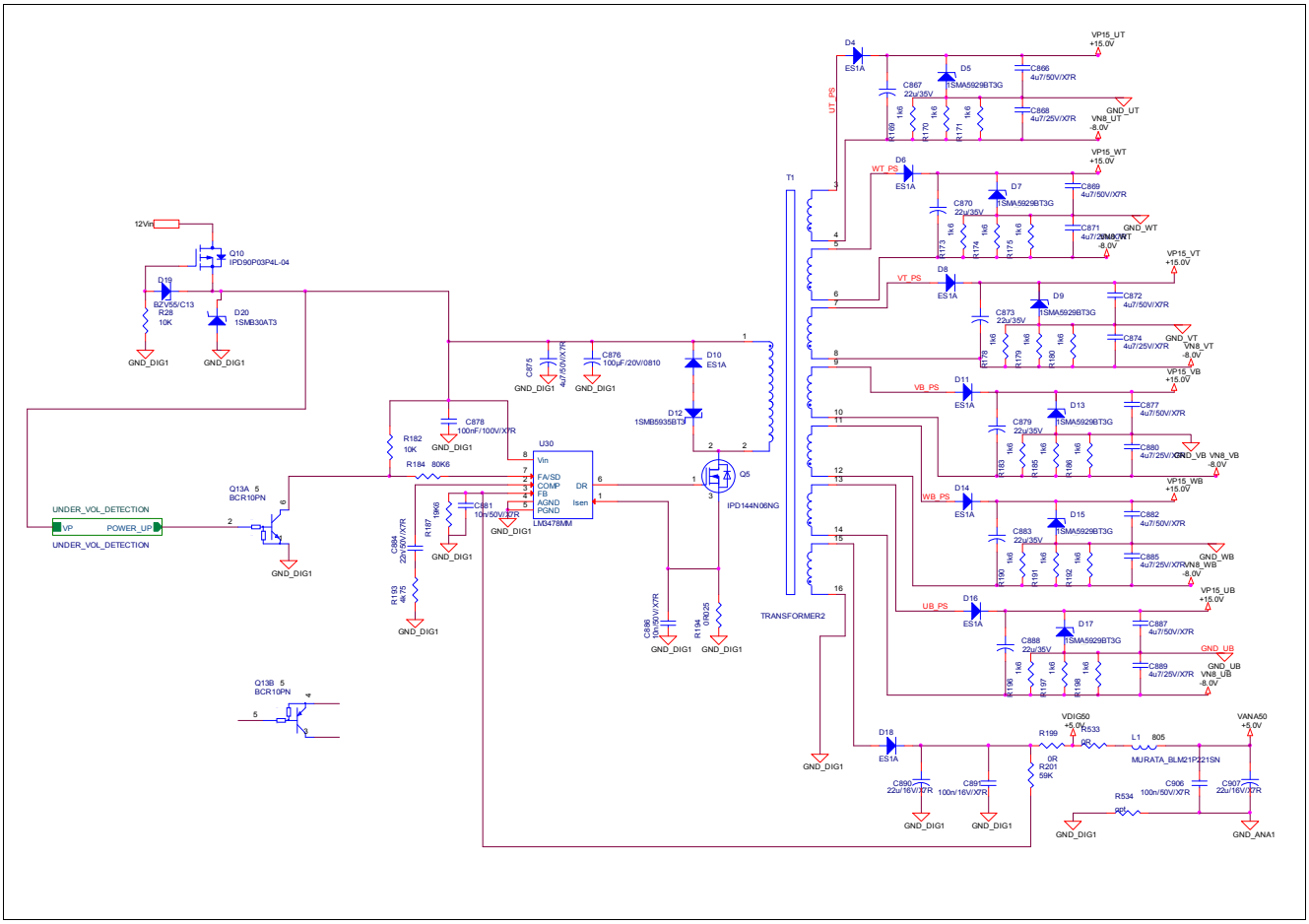


Figure 29 SMPS - Power Supply

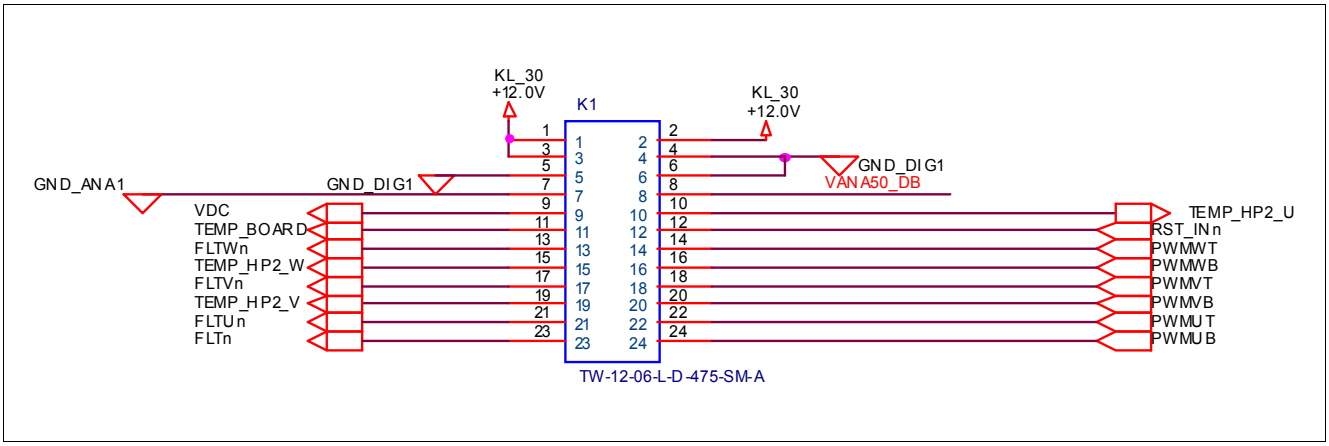


Figure 30 External Connector

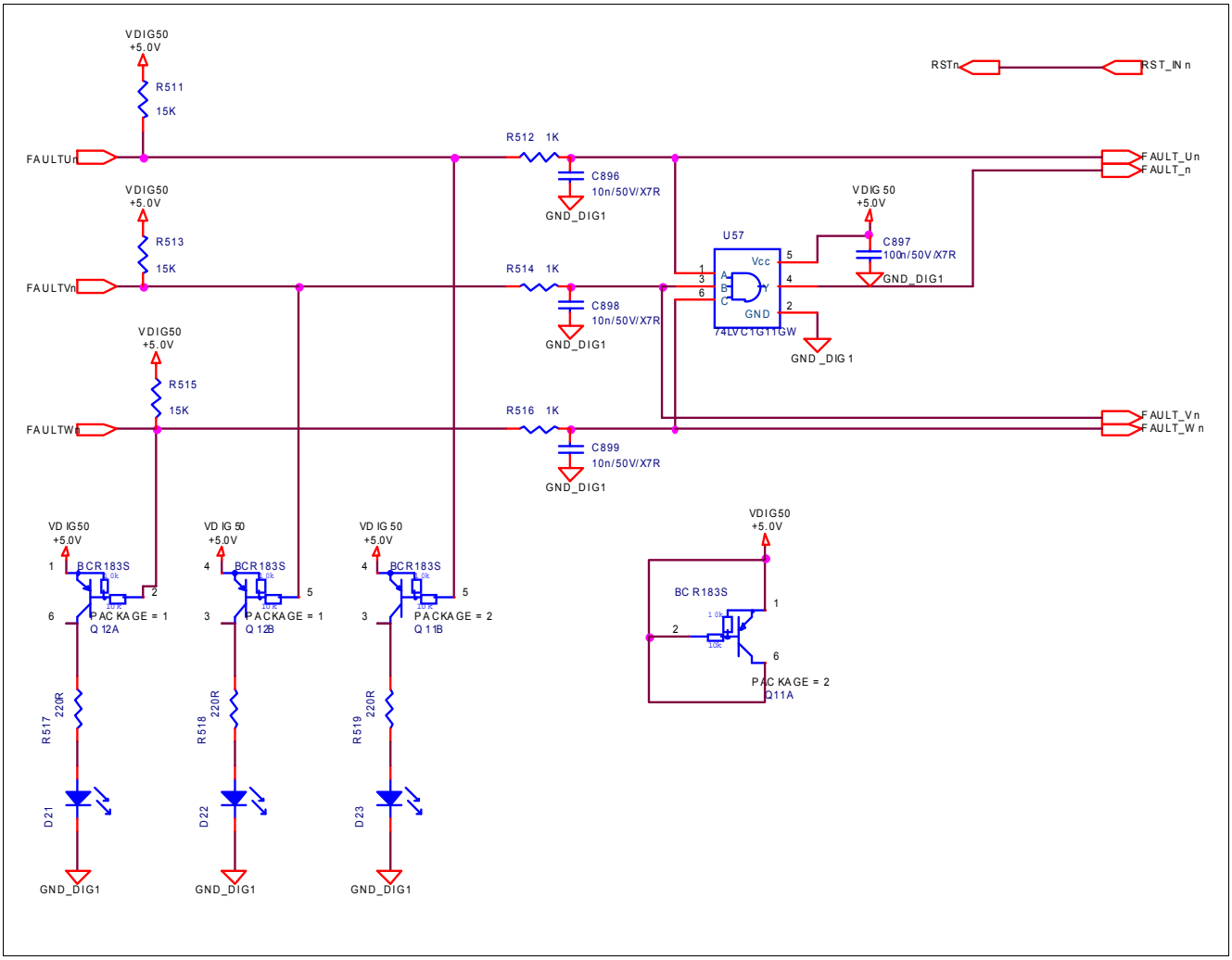


Figure 31 Fault Logic

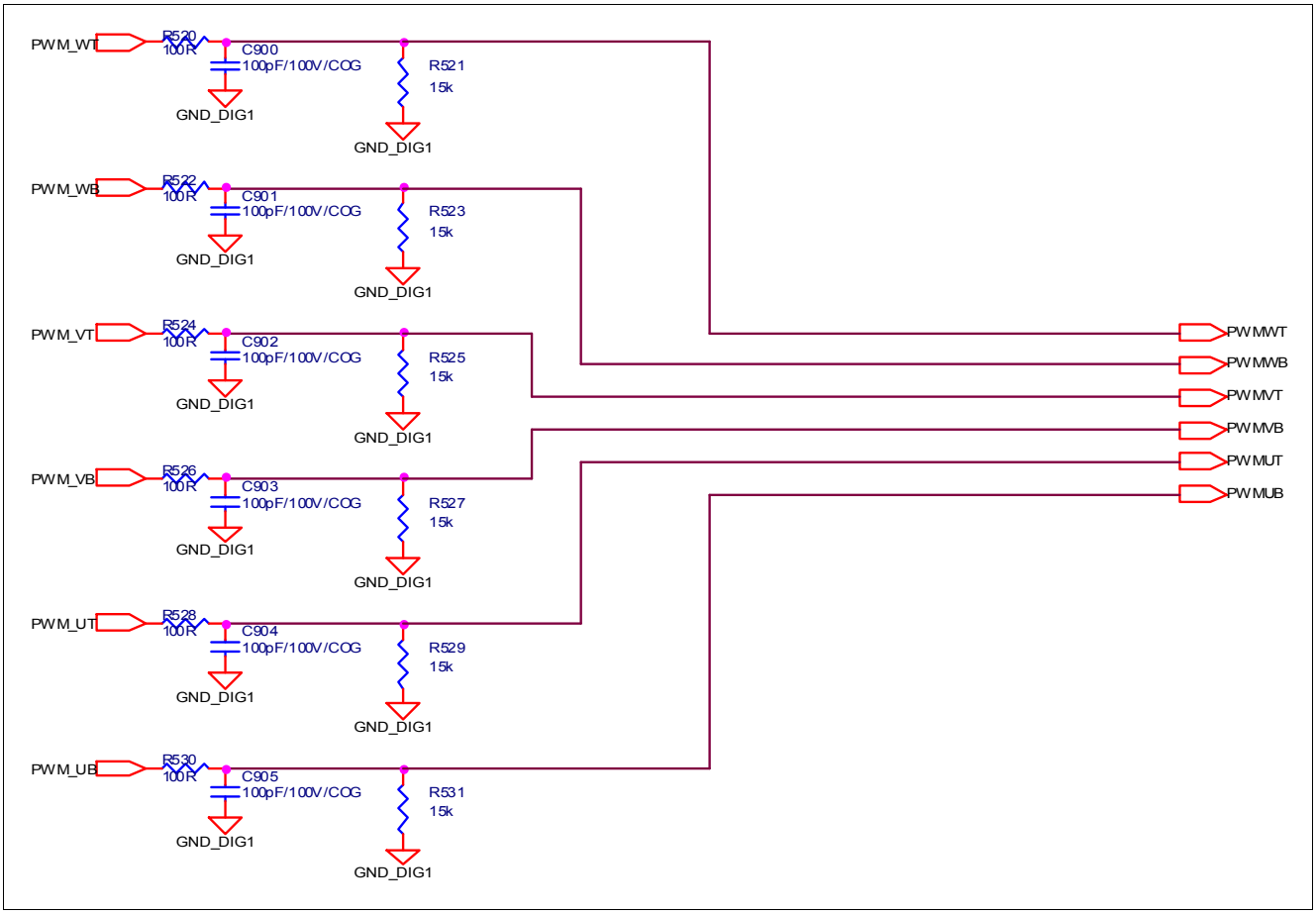


Figure 32 Input Logic

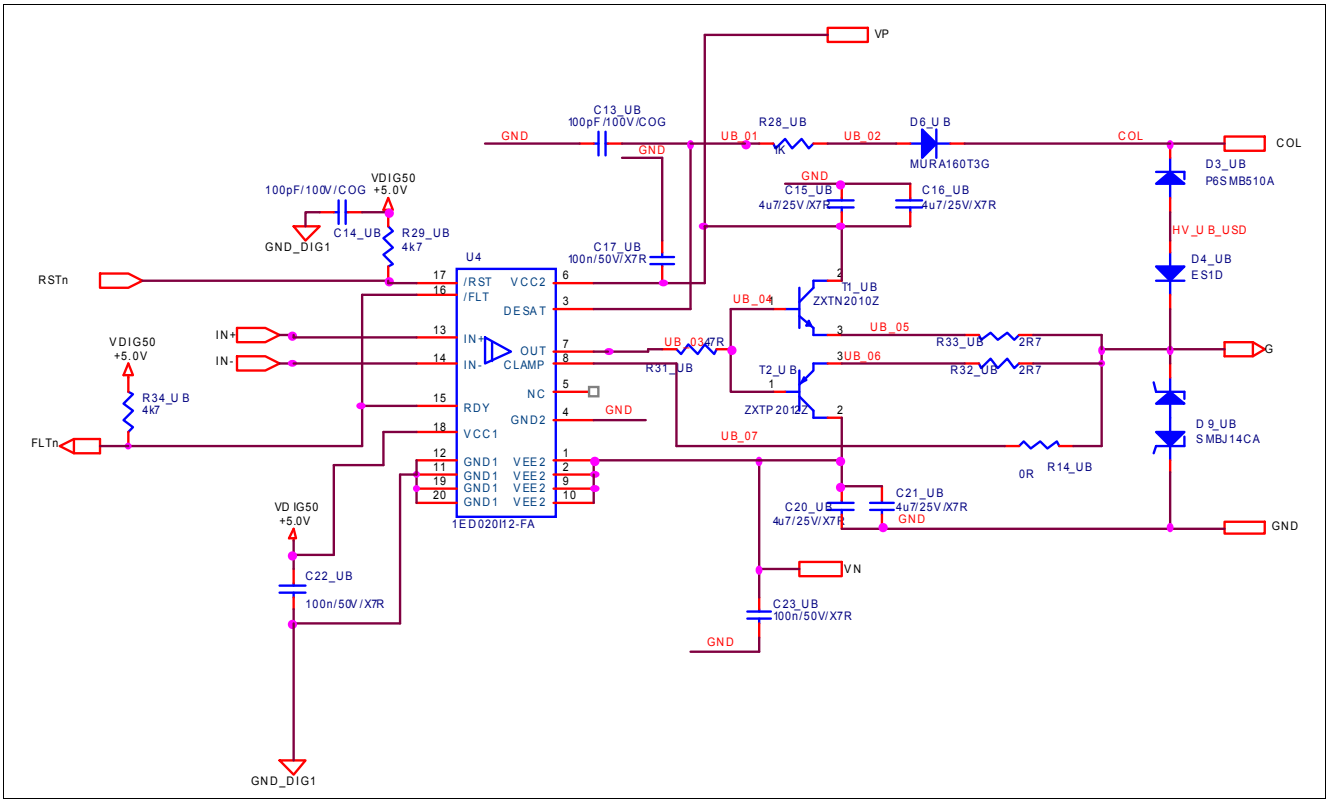


Figure 33 IGBT Driver - Bottom Transistor of Phase U

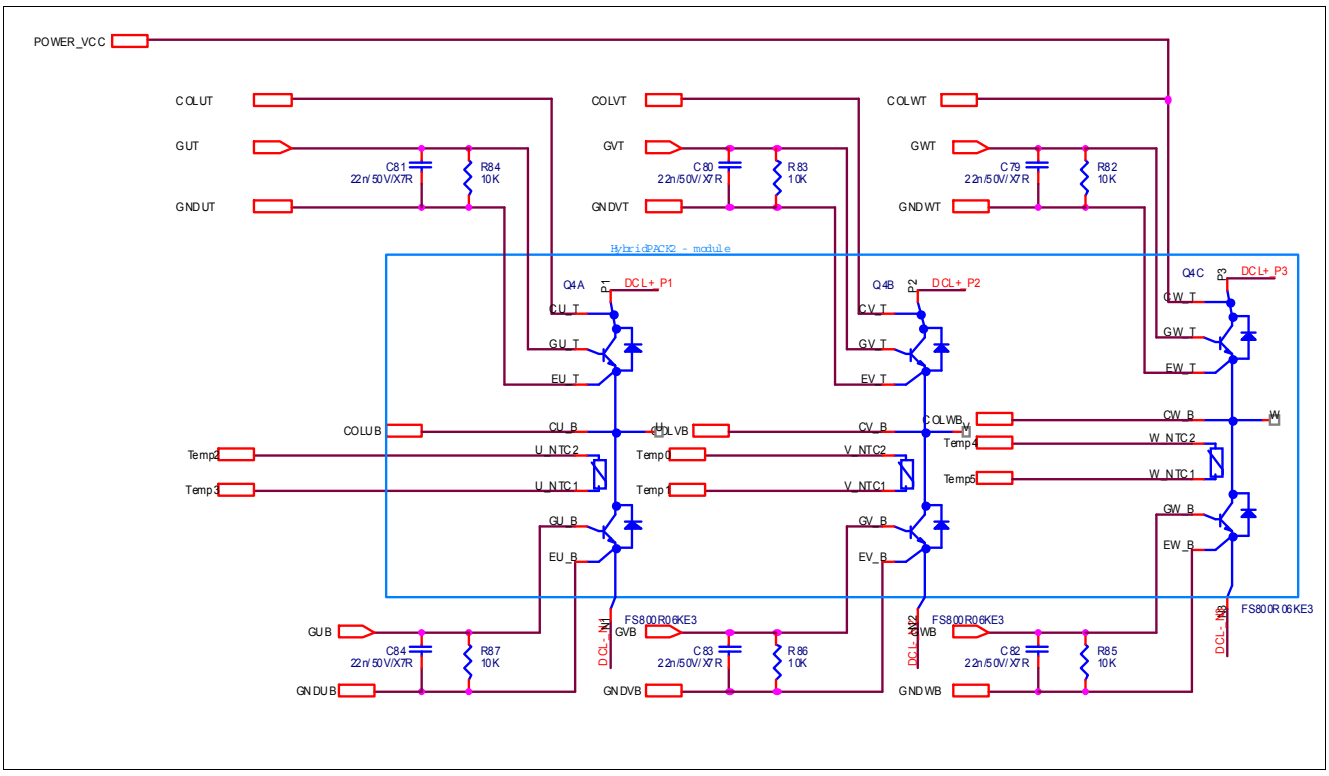


Figure 34 IGBT Module

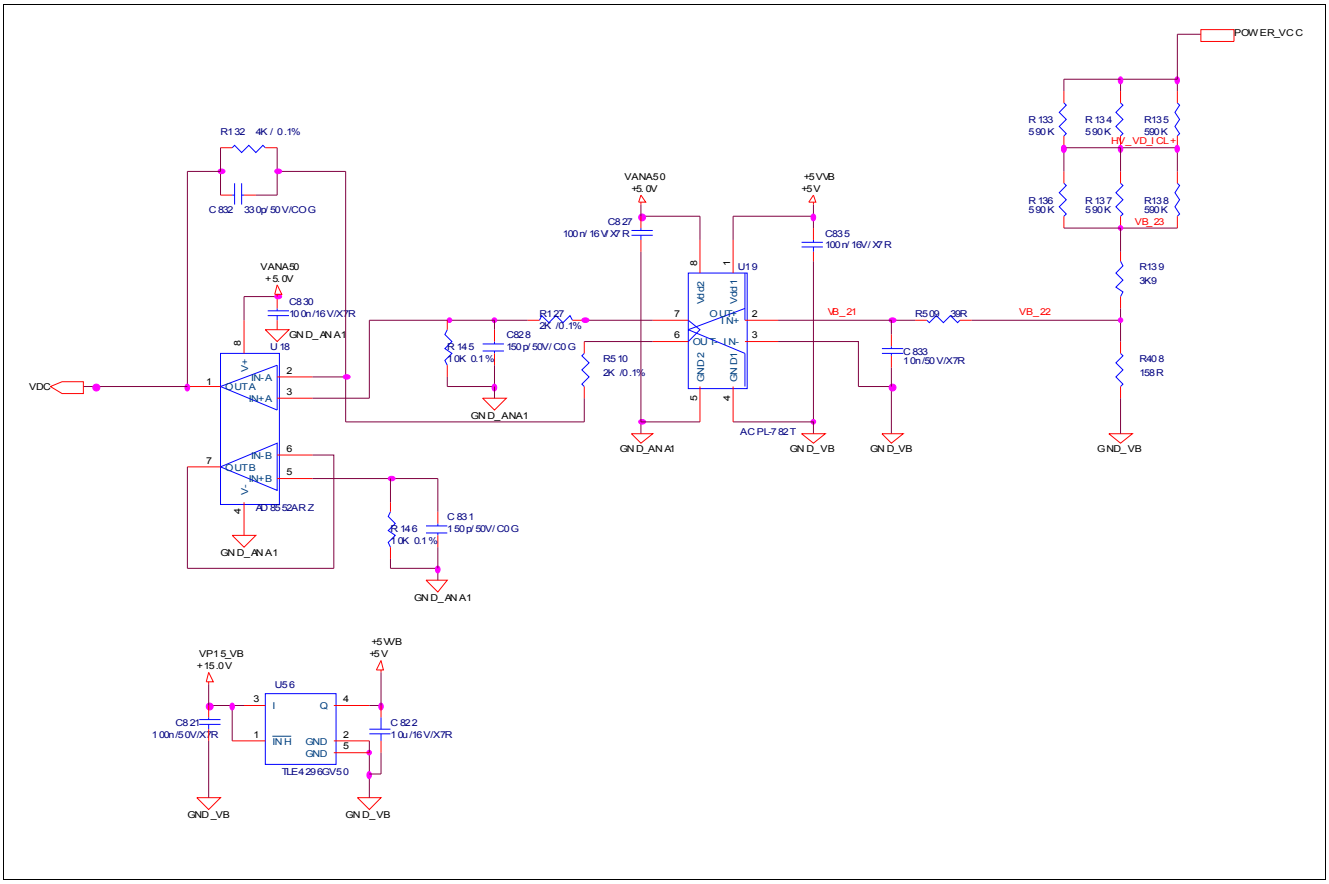


Figure 35 DC Voltage Measurement

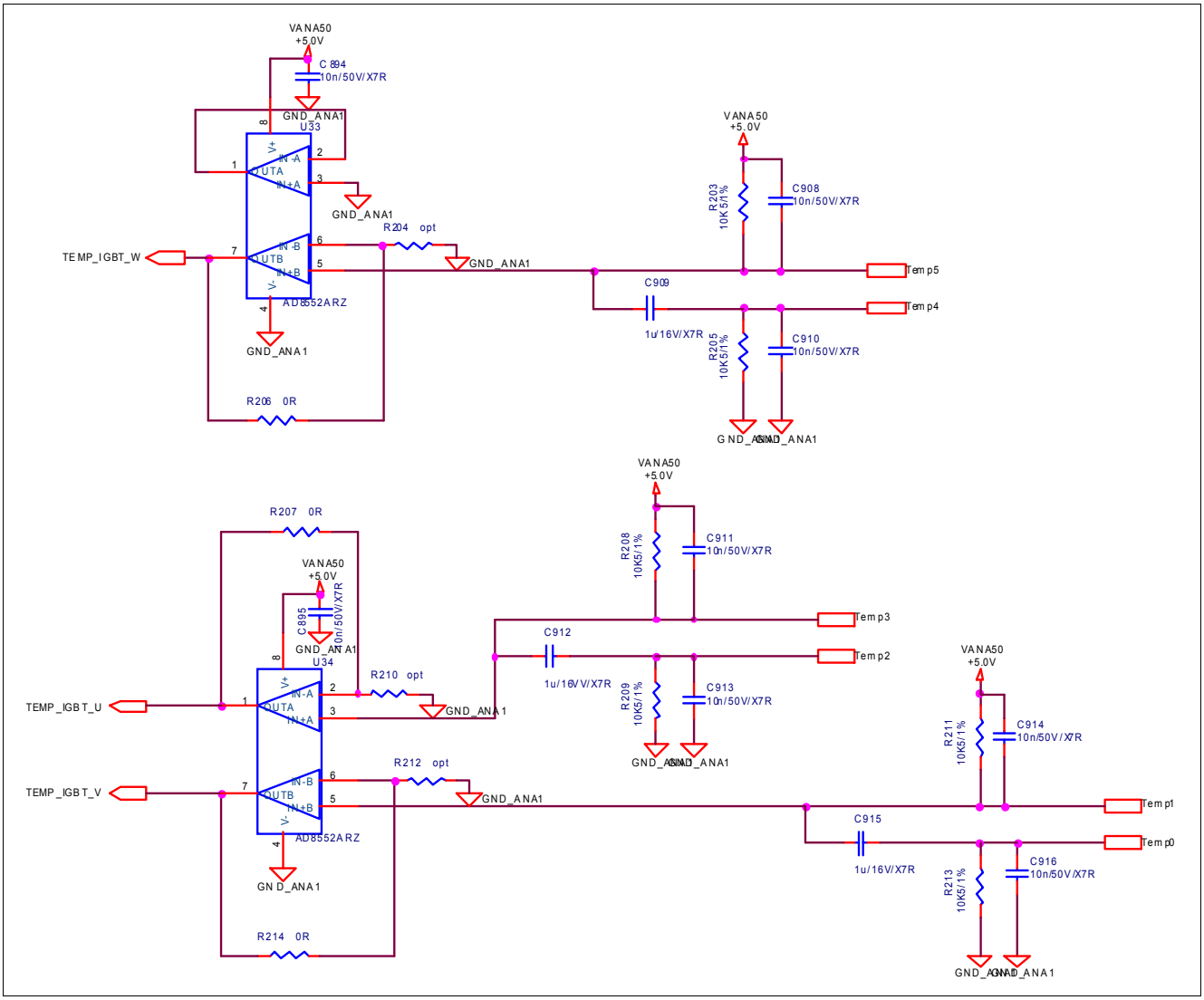


Figure 36 IGBT Module Temperature Measurement

3.8.2 Assembly Drawing

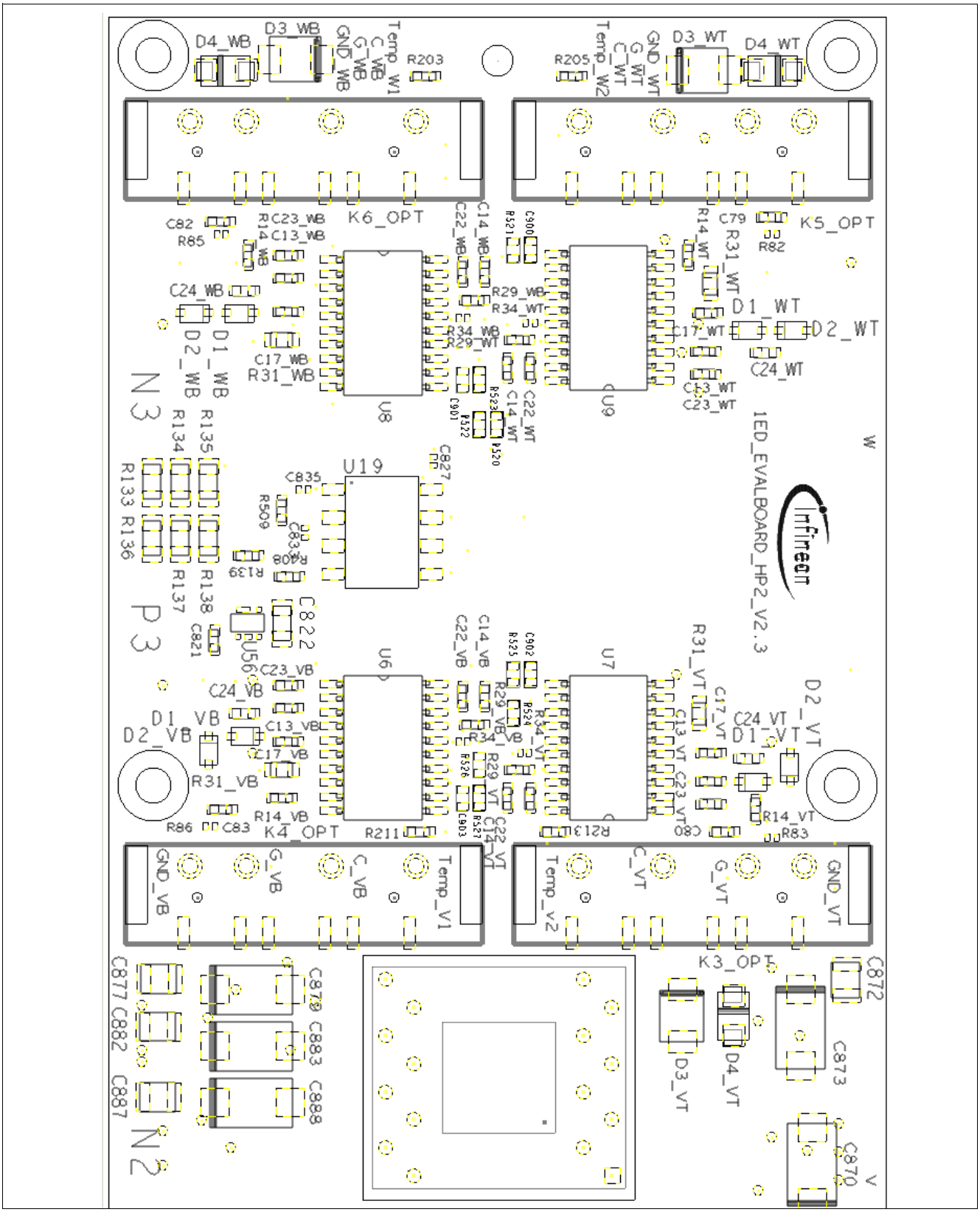


Figure 37 Assembly Drawing of the Driver Board (Top) - part 1

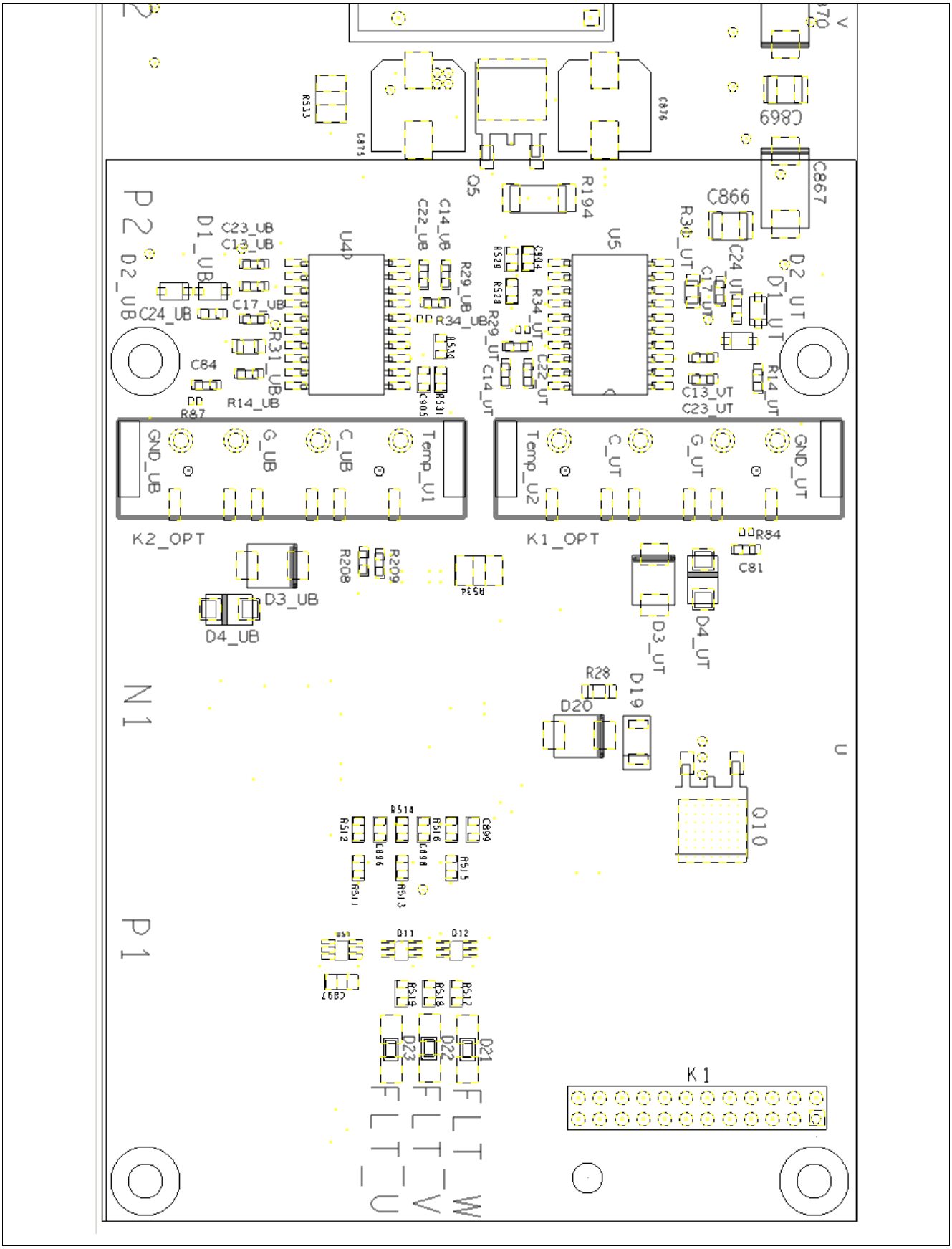


Figure 38 Assembly Drawing of the Driver Board (Top) - part 2

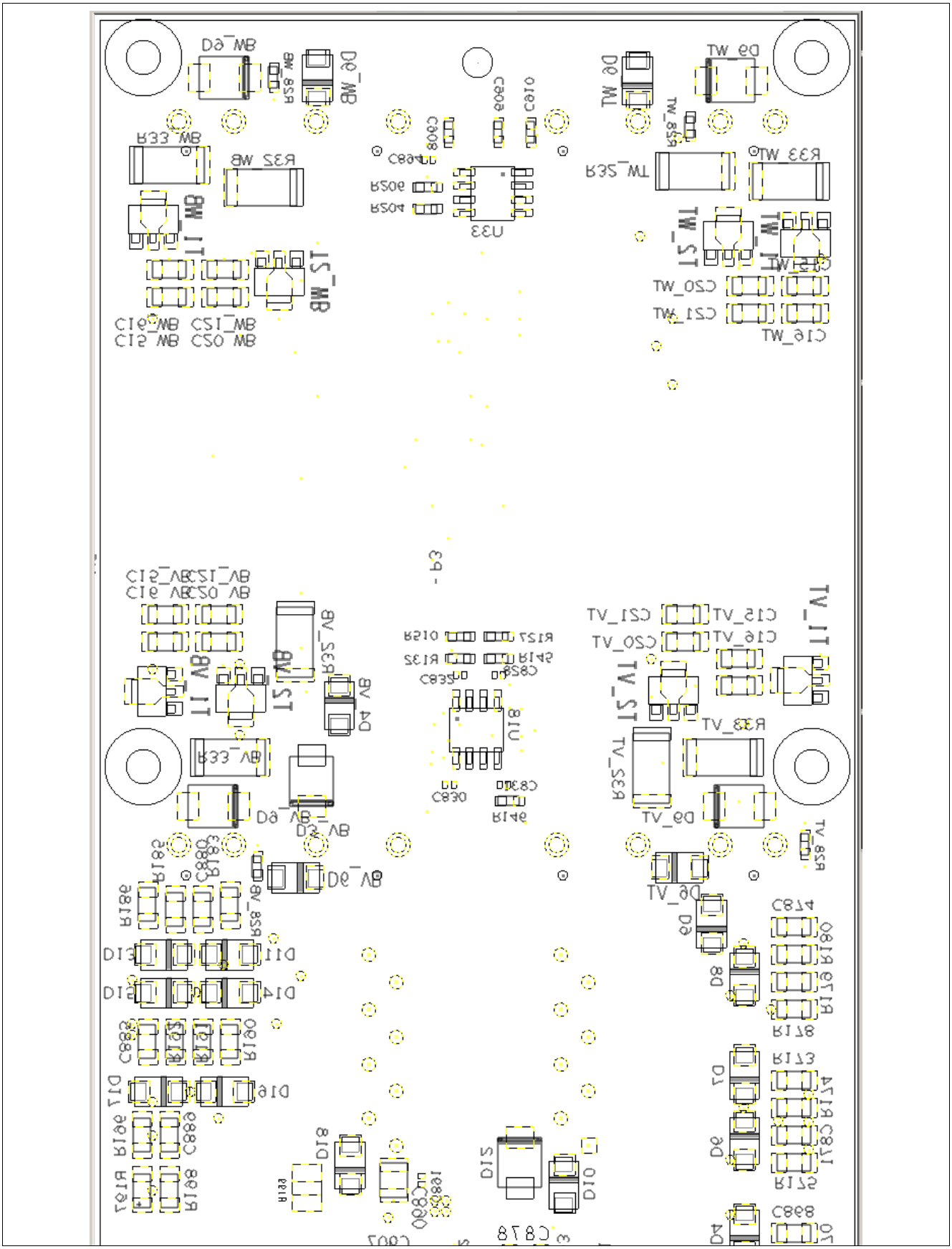


Figure 39 Assembly Drawing of the Driver Board (Bottom) - part 1

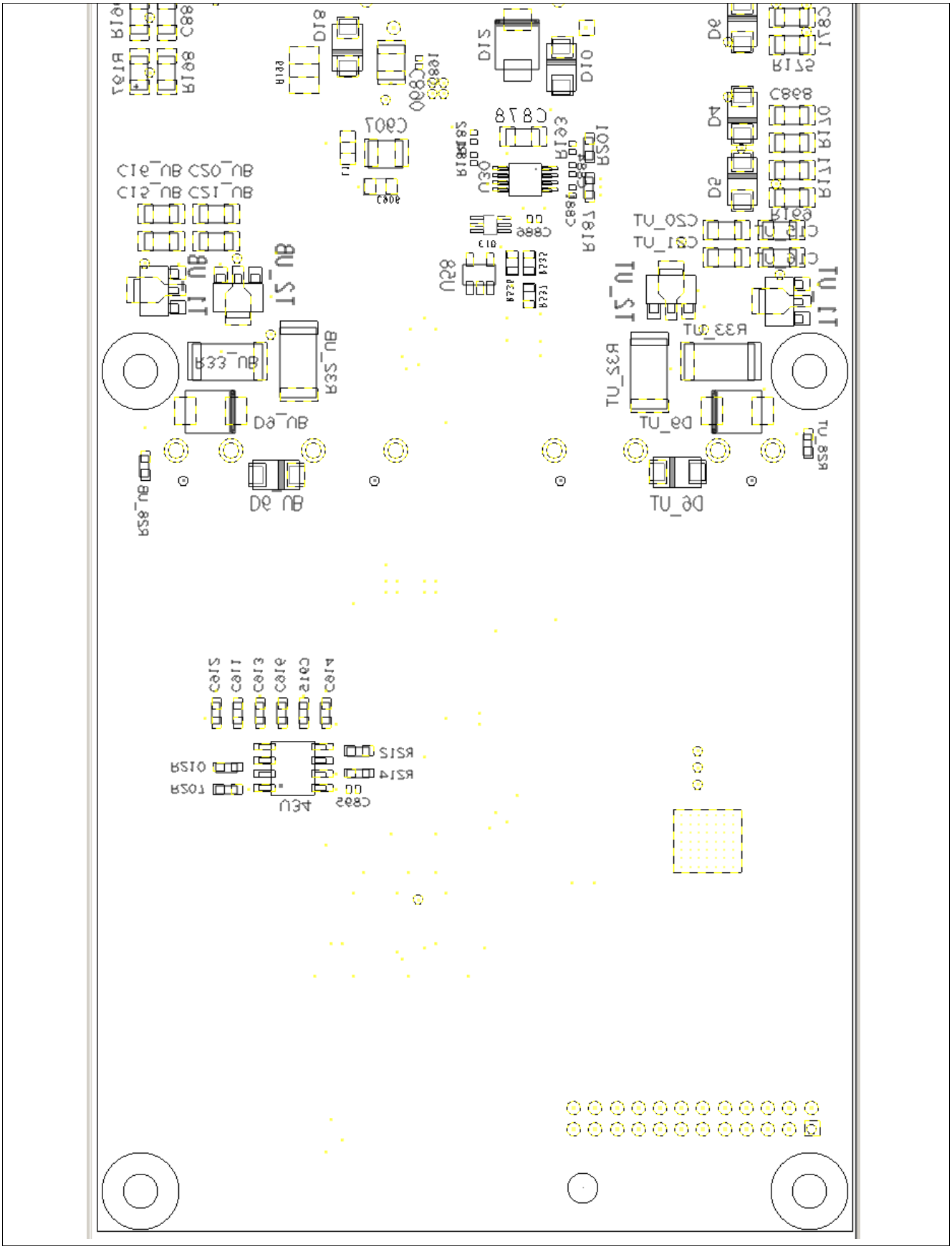


Figure 40 Assembly Drawing of the Driver Board (Bottom) - part 2

For detail information use the zoom function of your PDF viewer to zoom into the drawings on Figure 37, Figure 38, Figure 39 and Figure 40.

3.8.3 Layout

Layout of the Driver Board is shown on Figure 41 (Top Layer), on Figure 42 (Layer 2), on Figure 43 (Layer 3), on Figure 44 (Layer 4), on Figure 45 (Layer 5) and on Figure 46 (Bottom Layer).

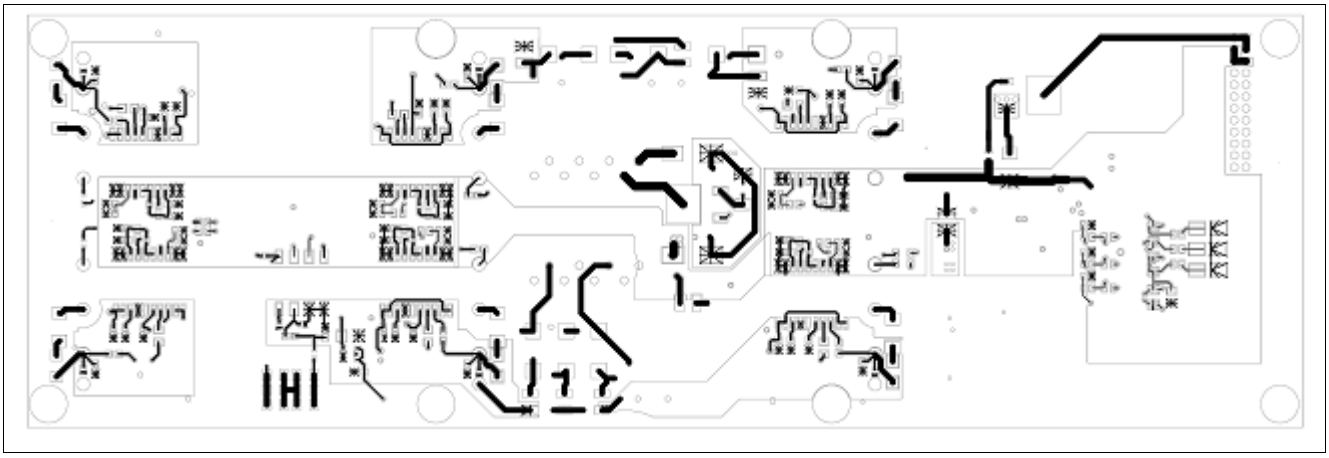


Figure 41 Driver Board - Top Layer

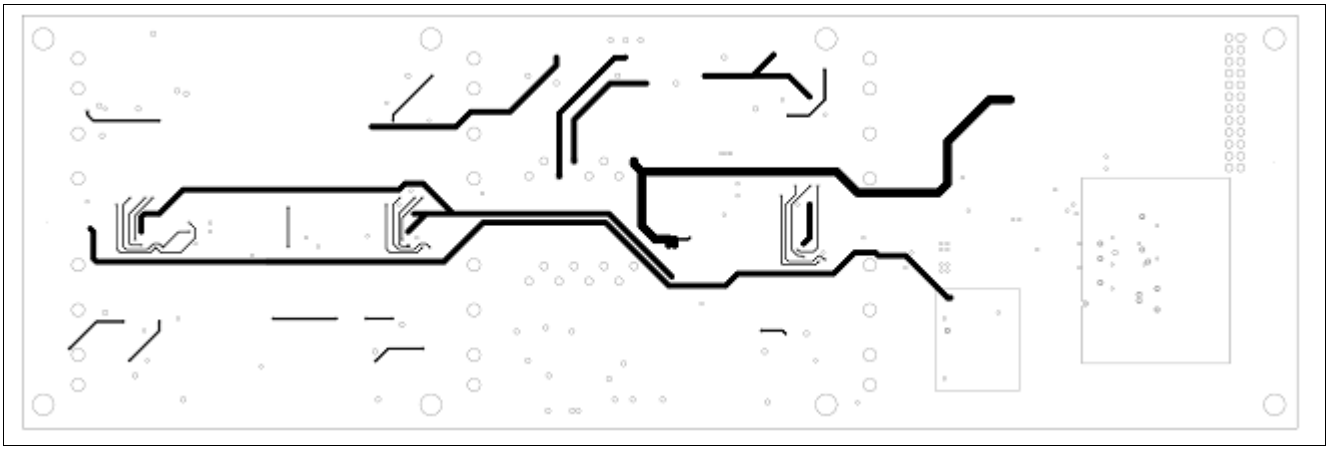


Figure 42 Driver Board - Layer 2

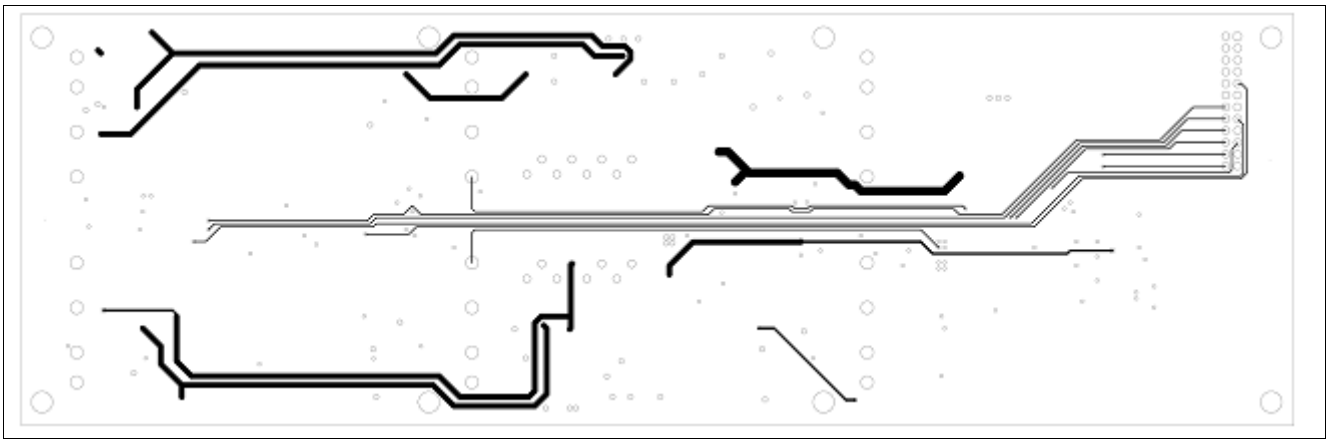


Figure 43 Driver Board - Layer 3

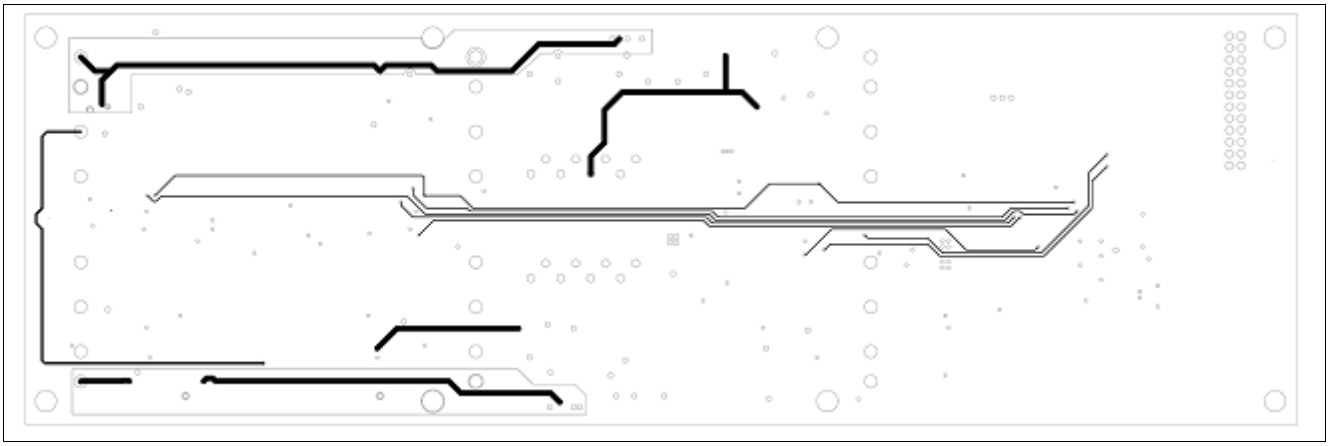


Figure 44 Driver Board - Layer 4

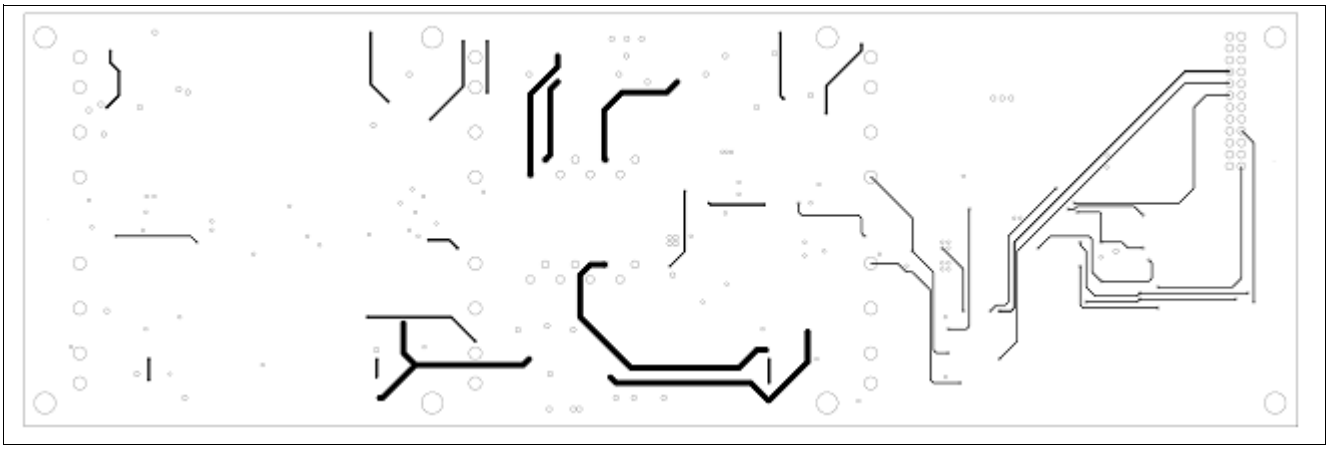


Figure 45 Driver Board - Layer 5

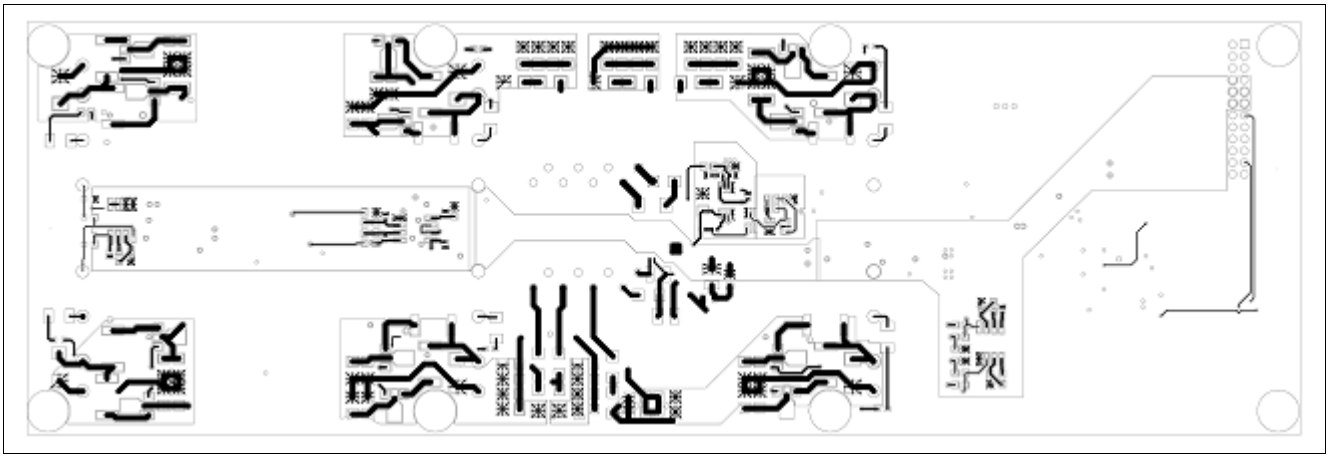


Figure 46 Driver Board - Bottom Layer

3.8.4 Bill of Materials

Table 3 Bill of Materials for Hybrid Kit for the HybridPACK™2 Evaluation Driver Board

Reference	Value / Device	Package
C15_WT,C15_WB,C15_VT,C15_VB,C15_UT, C15_UB,C16_WT,C16_WB,C16_VT,C16_VB, C16_UT,C16_UB,C20_WT,C20_WB,C20_VT, C20_VB,C20_UT,C20_UB,C21_WT,C21_WB, C21_VT,C21_VB,C21_UT,C21_UB,C868,C87 1,C874,C880,C885,C889	4u7/25V/X7R	C1206
C17_WT,C17_WB,C17_VT,C17_VB,C17_UT, C17_UB,C22_WT,C22_WB,C22_VT,C22_VB, C22_UT,C22_UB,C23_WT,C23_WB,C23_VT, C23_VB,C23_UT,C23_UB,C821	100n/50V/X7R	C0603
C79,C80,C81,C82,C83,C84	22n/50V/X7R	C0603
C822	10u/16V/X7R	C1206
C827,C830,C835,C891	100n/16V/X7R	C0402
C828,C831	150p/50V/C0G	C0402
C832	330p/50V/COG	C0402
C833,C881,C886,C894,C895	10n/50V/X7R	C0402
C866,C869,C872,C877,C882,C887	4u7/50V/X7R	C1210
C867,C870,C873,C879,C883,C888	22u/35V	EIA 7343-31 (Kemet D)
C875	4u7/50V/X7R	C1210
C876	100u/20V	C0810
C878	100nF/100V/X7R	C1206
C884	22n/50V/X7R	C0402
C890,C907	22u/16V/X7R	C1210
C896,C898,C899	10n/50V/X7R	C0603
C897,C906	100n/50V/X7R	C0805
C900,C901,C902,C903,C904,C905	100pF/100V/COG	C0603
C908,C910,C911,C913,C914,C916	10n/50V/X7R	C0603
C909,C915	1u/16V/X7R	C0603
C912	1u/16VV/X7R	C0603
D3_WT,D3_WB,D3_VT,D3_VB,D3_UT,D3_UB	P6SMB510A	SMB
D4,D6,D8,D10,D11,D14,D16,D18	ES1A	DO214
D4_WT,D4_WB,D4_VT,D4_VB,D4_UT,D4_UB	ES1D	DO214
D5,D7,D9,D13,D15,D17	1SMA5929BT3G	DO214
D6_WT,D6_WB,D6_VT,D6_VB,D6_UT,D6_UB	MURA160T3G	DO214
D9_WT,D9_WB,D9_VT,D9_VB,D9_UT,D9_UB	SMBJ14CA	SMB
D12	1SMB5935BT3	SMB
D19	BZV55/C13	SMD

Table 3 Bill of Materials for Hybrid Kit for the HybridPACK™2 Evaluation Driver Board (cont'd)

Reference	Value / Device	Package
D20	1SMB30AT3	SMB
D21,D22,D23	LED_LSM676-MQ	D0805
K1	MMS-112-01-L-DV	24POL
K1_opt,K2_opt,K3_opt,K4_opt,K5_opt,K6_opt	JST 09HVD6B-EMGF-NR	09HVD6B-EMGF-NR
L1	MURATA_BLM21P221SN	L0805
Q4	FS800R06KE3	HybridPACK™2
Q5	IPD144N06NG	TO252
Q10	IPD90P03P4L-04	TO252
Q11,Q12	BCR183S	SOT363
Q13	BCR10PN	SOT363
R14_WT,R14_WB,R14_VT,R14_VB,R14_UT, R14_UB,R206,R207,R214	0R	R0603
R28_WT,R28_WB,R28_VT,R28_VB,R28_UT, R28_UB	1K	R0603
R28	10K	R0805
R29_WT,R29_WB,R29_VT,R29_VB,R29_UT, R29_UB	4K7	R0603
R31_WT,R31_WB,R31_VT,R31_VB,R31_UT, R31_UB	47R	R0805
R32_WT,R32_WB,R32_VT,R32_VB,R32_UT, R32_UB,R33_WT,R33_WB,R33_VT,R33_VB, R33_UT,R33_UB	2R7	R2512
R34_WT,R34_WB,R34_VT,R34_VB,R34_UT, R34_UB,R193	4k75	R0402
R82,R83,R84,R85,R86,R87,R182	10K	R0402
R127,R510	2K /0.1%	R0603
R132	4K / 0.1%	R0603
R133,R134,R135,R136,R137,R138	590K	R1206
R139	3K9	R0603
R145,R146	10K 0.1%	R0603
R169,R170,R171,R173,R174,R175,R178,R179,R180,R183,R185,R186,R190,R191,R192,R196,R197,R198	1k6	R1206
R184	80K6	R0402
R187	19K6	R0603
R194	0R025	R2010
R199,R533	0R	R1210
R201	59K	R0603
R203,R205,R208,R209,R211,R213	10K/1%	R0603
R204,R210,R212	opt	R0603

Table 3 Bill of Materials for Hybrid Kit for the HybridPACK™2 Evaluation Driver Board (cont'd)

Reference	Value / Device	Package
R408	158R	R0603
R509	39R	R0603
R511,R513,R515,R521,R523,R525,R527,R529,R531	15k	R0603
R512,R514,R516	1K	R0603
R517,R518,R519	220R	R0603
R520,R522,R524,R526,R528,R530	100R	R0603
R534	opt	R1210
R535	226K	R0603
R536	5K1	R0603
R537	47K	R0603
T1	TRANSFORMER2	
T1_WT,T1_WB,T1_VT,T1_VB,T1_UT,T1_UB	ZXTN2010Z	SOT89
T2_WT,T2_WB,T2_VT,T2_VB,T2_UT,T2_UB	ZXTP2012Z	SOT89
U4,U5,U6,U7,U8,U9	1ED020I12-FA	PG-DSO-20
U18,U33,U34	AD8552ARZ	SO-8
U19	ACPL-782T	DIP-8
U30	LM3478MM	MSOP-8
U56	TLE4296GV50	SCT595
U57	74LVC1G11GW	SOT363
U58	MAX6457UKD3A-T	SOT23-5

4 Hybrid Kit for the HybridPACK™2 Logic Board

Logic Board contains all components for the control of the Hybrid Kit for the HybridPACK™2. Furthermore it provides the interface for all the others elements which build a complete inverter system: motor interface (encoder, resolver, GMR or hall sensor), current sense interface, communication (CAN and RS232) and additional analogue and digital inputs/outputs. It is supported in 2 versions: version v1.2 on **Figure 47** (not produced anymore) and version v1.3b on **Figure 48**. **Figure 49** shows the block structure of the Logic Board and the following chapters describe these blocks in detail. Although the block structure shown on **Figure 49** can be applied on both versions, v1.2 and v1.3b are different in a few details. Comparing to v1.2 the Logic Board v1.3b is a further step in the development of the Hybrid Kit that offers some new features to the customer - the most important is GMR interface detailed described in **Chapter 4.10**.

New features on Logic Board v1.3b comparing to v1.2 are following:

- On-Board (on the bottom of the Logical Board) temperature measurements (**Figure 78**);
- Usage of Infineon Technologies TLE7368E Micro Controller Power Supply IC (**Figure 63**);
- Added some reference power supply for MCU A/D converters;
- Implemented parallel communication interface on resolver chip AD2S1200YST (IC8 on **Figure 67**) and added belonging circuitry (see **Figure 69**);
- Added more options for trimming the resolver signal and added test points for measuring resolver signals;
- Implemented differential signaling to the encoder interface (instead of single ended interface as it was in v1.2);
- Improved phase current sense filtering - adapted to filter signals up to 5kHZ cut-off frequency by means of second order filter (**Figure 74**);
- Adapted filtering on DC-Bus voltage measuring signals, temperature sensing signals, emulated encoder outputs of resolver chip (**Figure 74**);
- Removed one general purpose digital I/O due to leak of pins on the connector;
- Due to added differential signaling and GMR interface the external interface 34-pin connector is replaced with 50-pin connector; (**Figure 50** and **Figure 51**);

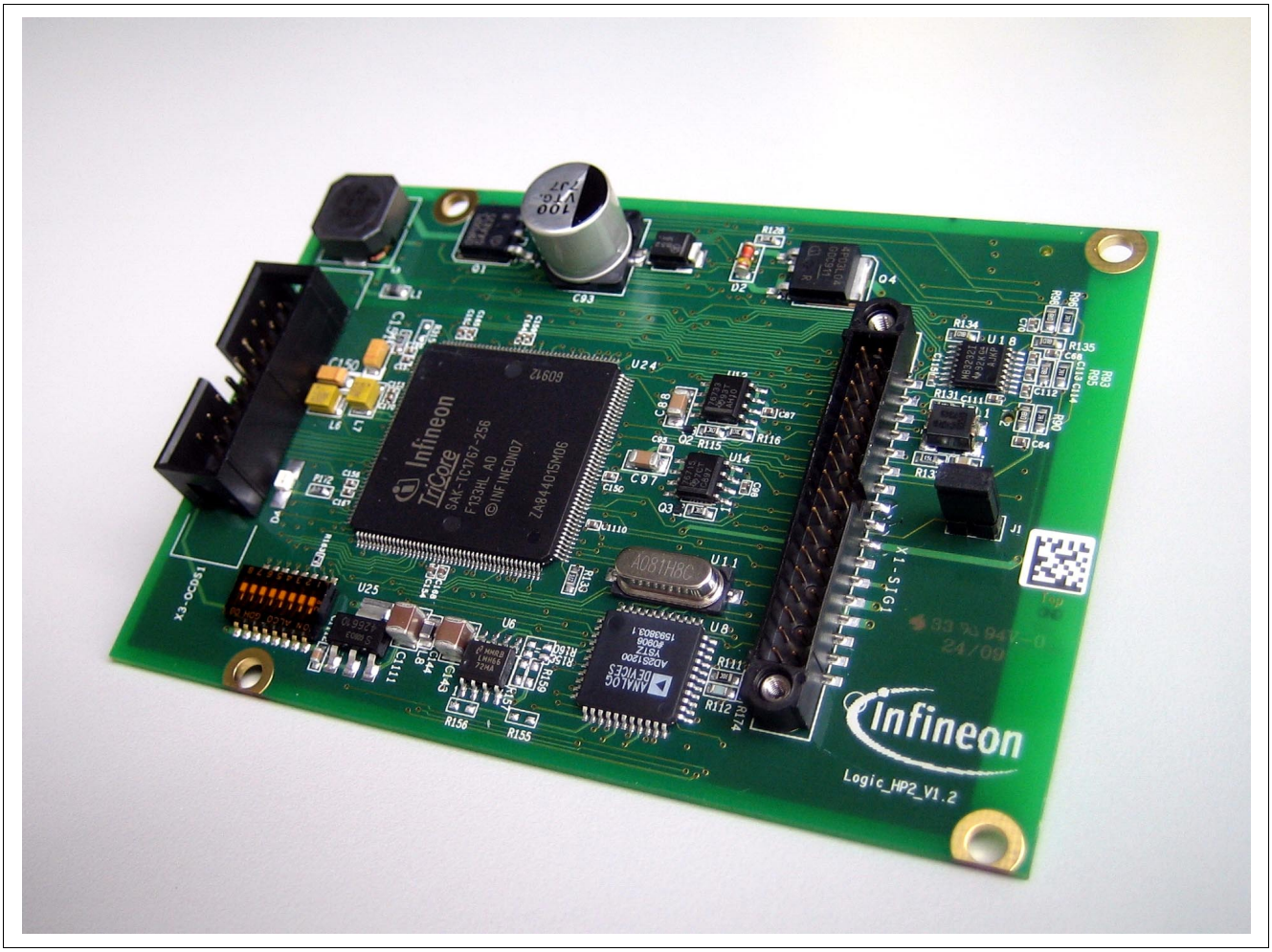


Figure 47 Hybrid Kit for the HybridPACK™2 Logic Board v1.2

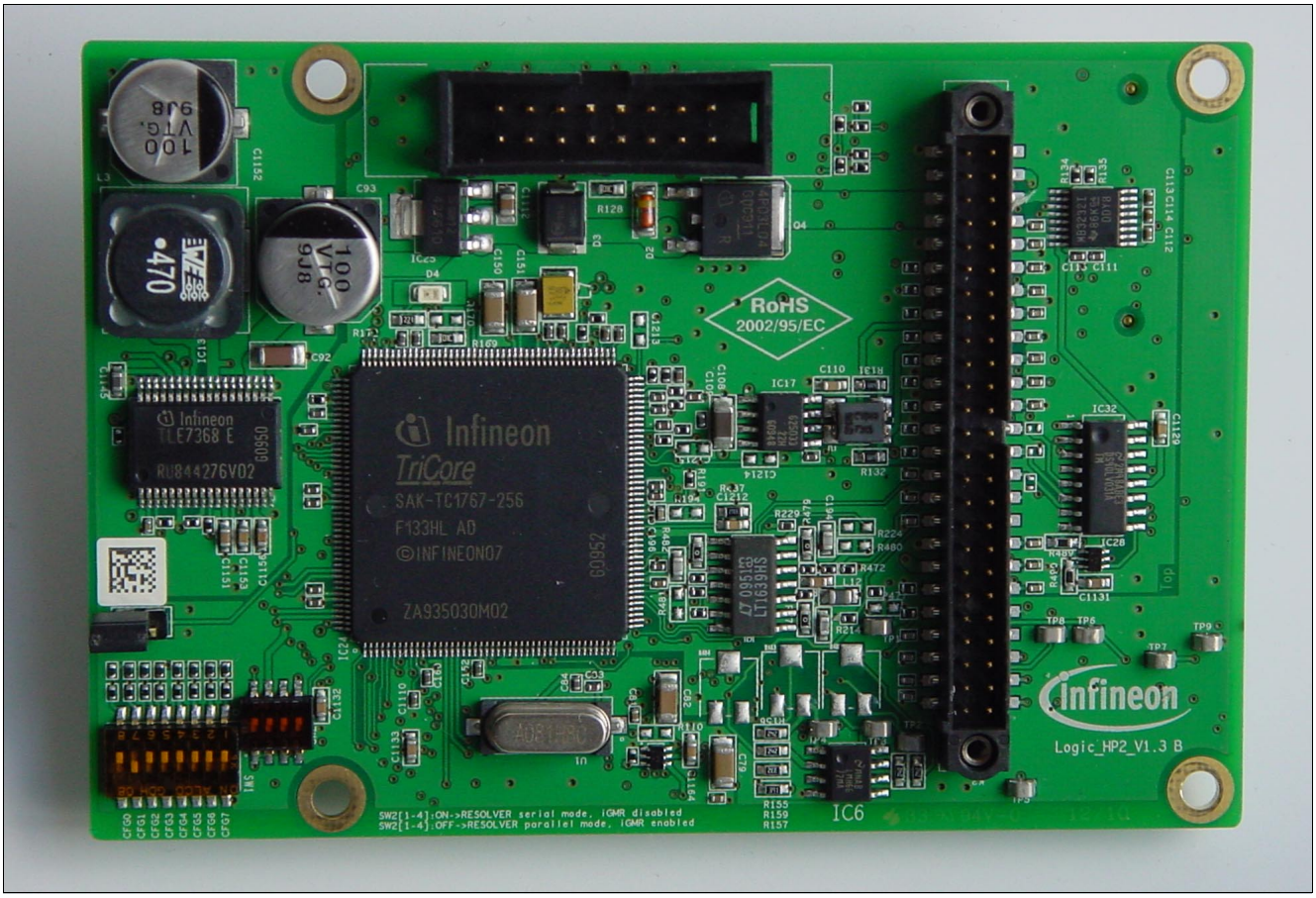


Figure 48 Hybrid Kit for the HybridPACK™2 Logic Board v1.3b

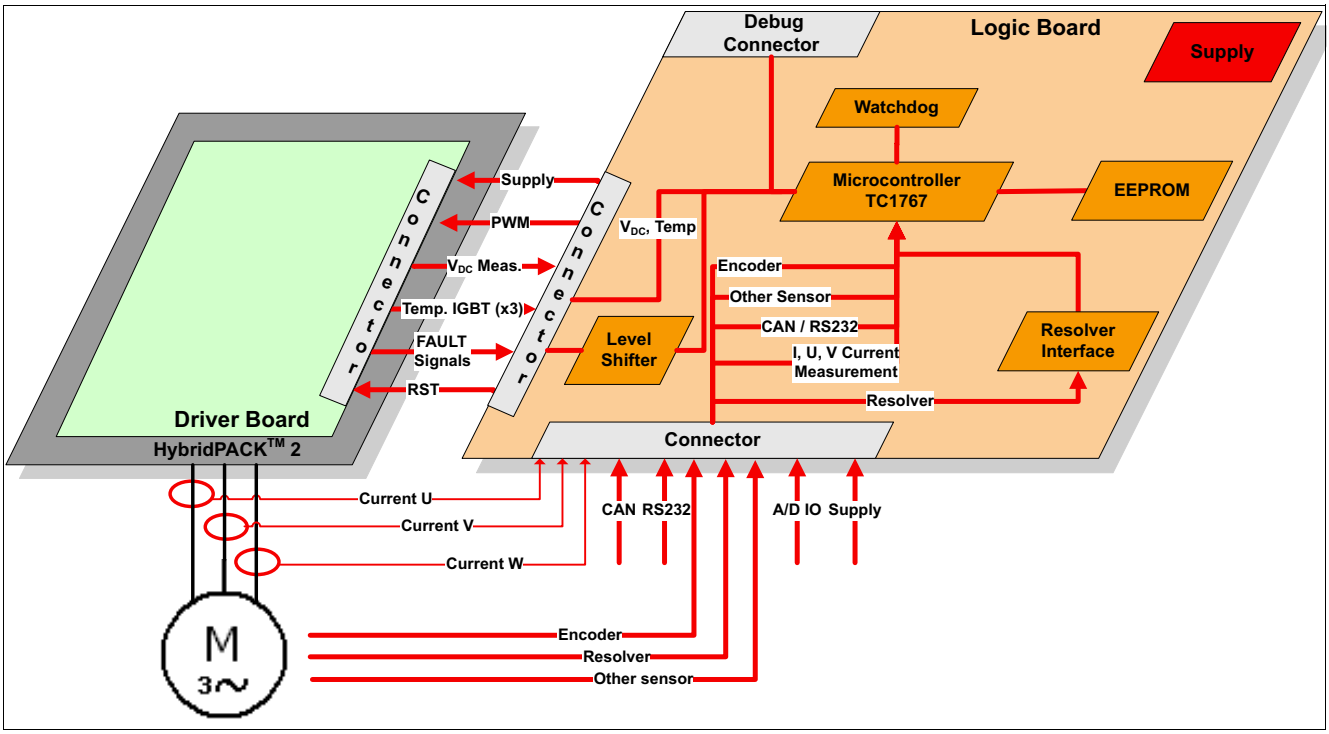


Figure 49 Block Diagram of the Logic Board

4.1 External Connector Pin Assignment

Logic Board external connector X1-SIG1 (Harwin M80-5123442 on Logic Board v1.2) or K2 (Harwin M80-5125042P on Logic Board v1.3b) provides the interface to all the external systems: motor (encoder, resolver, Hall sensor or GMR), current sense, communication (CAN and RS232) and extra analogue and digital inputs/outputs. **Figure 50** and **Table 4** are showing the pin assignment of the connector X1-SIG1 for the Logic Board v1.2. **Figure 51** and **Table 5** are showing the pin assignment of the connector K2 for the Logic Board v1.3b. The female part for 34-pin connector Harwin M80-5123442 (Logic Board v1.2) is socket Harwin M80-4603442. The female part for 50-pin connector Harwin M80-5125042P (Logic Board v1.3b) is socket Harwin M80-4605042.

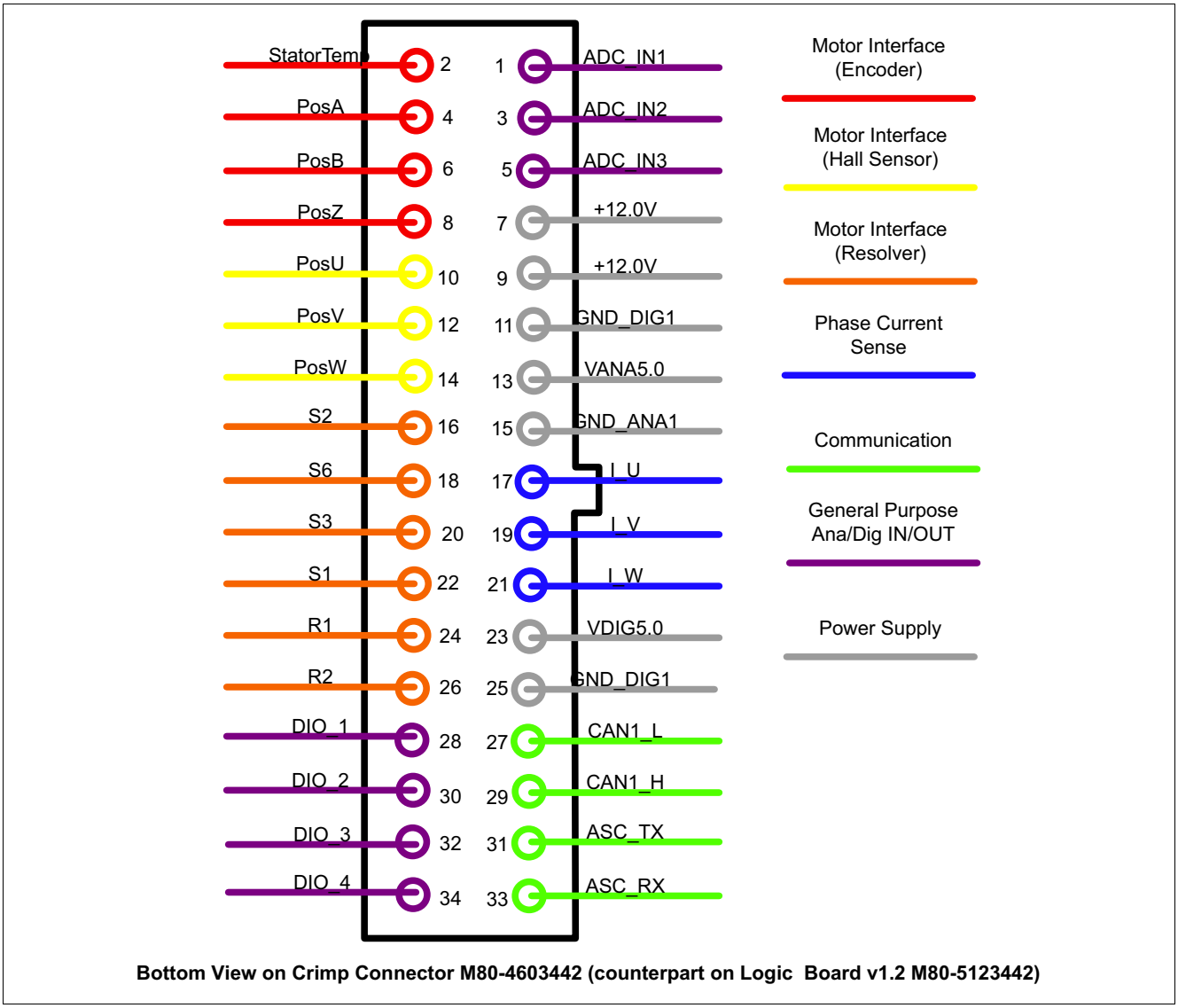


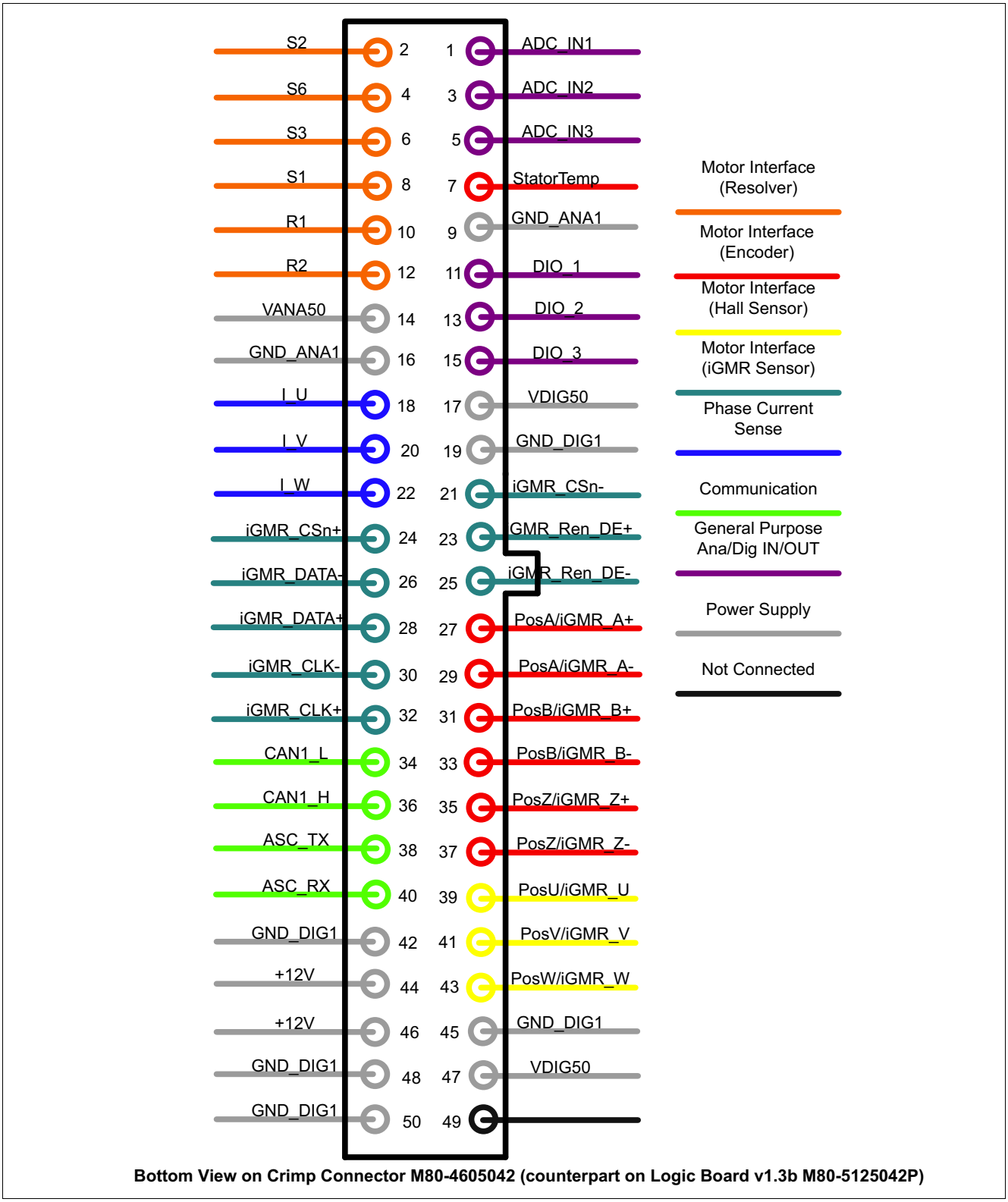
Figure 50 External Connector Pin Assignment Logic Board v1.2

Table 4 External Connection Pin Assignment Logic Board v1.2

Pin Number	Pin Name	Type	Description
1	ADC_IN1	I/O	General Purpose Analog I/O
2	StatorTemp	Input	Motor Temperature Measurement
3	ADC_IN2	I/O	General Purpose Analog I/O
4	PosA	Input	Encoder Phase A

Table 4 External Connection Pin Assignment Logic Board v1.2

Pin Number	Pin Name	Type	Description
5	ADC_IN3	I/O	General Purpose Analog I/O
6	PosB	Input	Encoder Phase B
7	KL_30_IN	Supply	+12.0V Power Supply
8	PosZ	Input	Encoder Phase Z - index
9	KL_30_IN	Supply	+12.0V Power Supply
10	PosU	Input	Hall Sensor Phase U
11	GND_DIG1	Supply	Digital Ground
12	PosV	Input	Hall Sensor Phase V
13	VANA50	Supply	+5.0V Analog Power Supply
14	PosW	Input	Hall sensor Phase W
15	GND_ANA1	Supply	Analog Ground
16	S2	Input	Resolver Sine (high)
17	I_U	Input	Current Sense Phase U
18	S6	Input	Resolver Sine (low)
19	I_V	Input	Current Sense Phase V
20	S3	Input	Resolver Cosine (high)
21	I_W	Input	Current Sense Phase W
22	S1	Input	Resolver Cosine (low)
23	VDIG50	Supply	+5.0V Digital Power Supply
24	R1	Output	Resolver Excitation (high)
25	GND_DIG1	Supply	Digital Ground
26	R2	Output	Resolver Excitation (low)
27	CAN1_L	I/O	Low line I/O CAN Signal
28	DIO1	I/O	General Purpose Digital I/O
29	CAN1_H	I/O	High line I/O CAN Signal
30	DIO2	I/O	General Purpose Digital I/O
31	ASC_TX	Output	RS-232 Transmitter Output
32	DIO3	I/O	General Purpose Digital I/O
33	ASC_RX	Input	RS-232 Receiver Input
34	DIO4	I/O	General Purpose Digital I/O



Bottom View on Crimp Connector M80-4605042 (counterpart on Logic Board v1.3b M80-5125042P)

Figure 51 External Connector Pin Assignment Logic Board v1.3b

Table 5 External Connector Pin Assignment Logic Board v1.3b

Pin Number	Pin Name	Type	Description
1	ADC_IN1	I/O	General Purpose Analog I/O
2	S2	Input	Resolver Sine (high)
3	ADC_IN2	I/O	General Purpose Analog I/O
4	S6	Input	Resolver Sine (low)
5	ADC_IN3	I/O	General Purpose Analog I/O
6	S3	Input	Resolver Cosine (high)
7	StatorTemp	Input	Motor Temperature Measurement
8	S1	Input	Resolver Cosine (low)
9	GND_ANA1	Supply	Analog Ground
10	R1	Output	Resolver Excitation (high)
11	DIO1	I/O	General Purpose Digital I/O
12	R2	Output	Resolver Excitation (low)
13	DIO2	I/O	General Purpose Digital I/O
14	VANA50	Supply	+5.0V Analog Power Supply
15	DIO3	I/O	General Purpose Digital I/O
16	GND_ANA1	Supply	Analog Ground
17	VDIG50	Supply	+5.0V Digital Power Supply
18	I_U	Input	Current Sense Phase U
19	GND_DIG1	Supply	Digital Ground
20	I_V	Input	Current Sense Phase V
21	iGMR_CSn-	Output	iGMR Chip Select (differential signal)
22	I_W	Input	Current Sense Phase W
23	iGMR_REn_DE+	Output	iGMR Read Enable (differential signal)
24	iGMR_CSn+	Output	iGMR Chip Select (differential signal)
25	iGMR_REn_DE-	Output	iGMR Read Enable (differential signal)
26	iGMR_DATA-	I/O	iGMR Data (differential signal)
27	PosA/iGMR_A+	Input	Encoder Phase A (differential signal)
28	iGMR_DATA+	I/O	iGMR Data (differential signal)
29	PosA/iGMR_A-	Input	Encoder Phase A (differential signal)
30	iGMR_CLK-	Output	iGMR SSC Clock (differential signal)
31	PosB/iGMR_B+	Input	Encoder Phase B (differential signal)
32	iGMR_CLK+	Output	iGMR SSC Clock (differential signal)
33	PosB/iGMR_B-	Input	Encoder Phase B (differential signal)
34	CAN1_L	I/O	Low line I/O CAN Signal
35	PosZ/iGMR_Z+	Input	Encoder Phase Z - index (differential signal)
36	CAN1_H	I/O	High line I/O CAN Signal
37	PosZ/iGMR_Z-	Input	Encoder Phase Z - index (differential signal)
38	ASC_TX	Output	RS-232 Transmitter Output

Table 5 External Connector Pin Assignment Logic Board v1.3b

Pin Number	Pin Name	Type	Description
39	PosU/iGMR_U	Input	Hall Sensor Phase U
40	ASC_RX	Input	RS-232 Receiver Input
41	PosV/iGMR_V	Input	Hall Sensor Phase V
42	GND_DIG1	Supply	Digital Ground
43	PosW/iGMR_W	Input	Hall Sensor Phase W
44	KL_30_IN	Supply	+12.0V Power Supply
45	GND_DIG1	Supply	Digital Ground
46	KL_30_IN	Supply	+12.0V Power Supply
47	VDIG50	Supply	+5.0V Digital Power Supply
48	GND_DIG1	Supply	Digital Ground
49	NC	NC	Not Connected
50	GND_DIG1	Supply	Digital Ground

4.2 Connector to the Driver Board (K1)

See **Chapter 3.3**.

4.3 Power Supply

The complete system (Driver Board and Logic Board) must to be supplied with and external DC power supply connected to connector X1-SIG1 on the Logic Board v1.2 or K2 on the Logic Board. On the Logic Board v1.2 +12V power supply should be connected to the pins 7 and 9 of X1-SIG1 and GND_DIG1 on pins 11 and 25 of X1-SIG1. On the Logic Board v1.3b +12V power supply should be connected to the pins 44 and 46 of K2 and GND_DIG1 on pins 19, 42, 45, 48 and 50 of K2. The input voltage should be kept between 7V and 18V and the current consumption will vary depending on different factors, i.e. PWM frequency.

This supply line will be forwarded to the Driver Board through the connector K1 (pins 1, 2 and 3 for +12V). On both boards a protection circuit will avoid damages in the case of overvoltage or wrong polarity (see **Figure 52**).

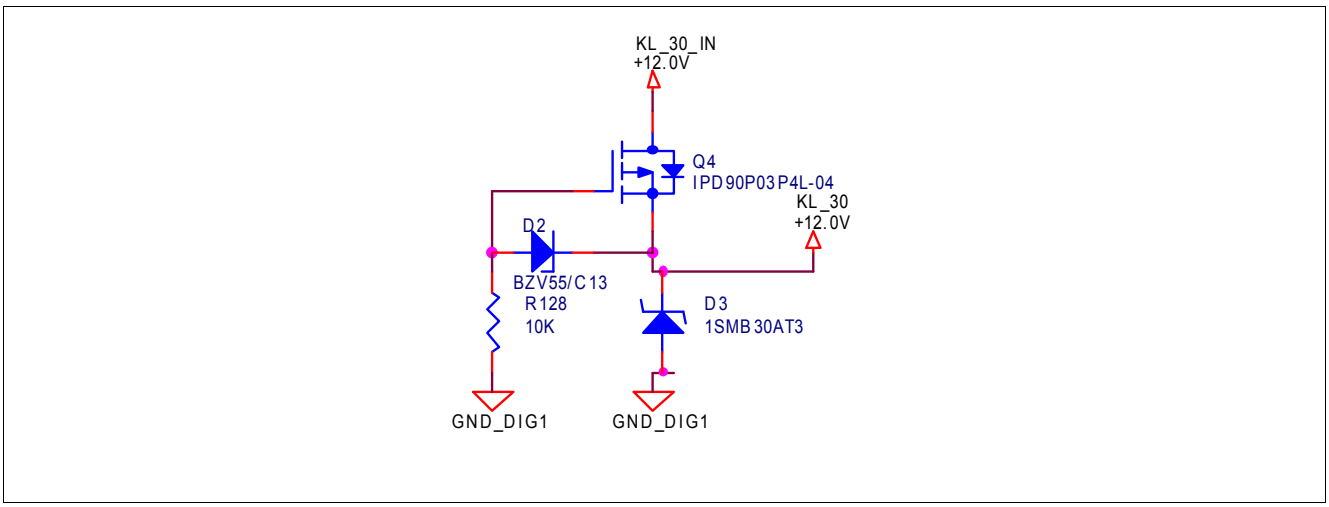


Figure 52 Overvoltage and Wrong Polarity Protection Circuit (same for Logic Board v1.2 and v1.3b)

The supply block (see **Figure 62** for Logic Board v1.2 and **Figure 63** for Logic Board v1.3b) generates all necessary voltages for the components on the logic board (5V, 3.3V and 1.5V). Furthermore the 5V (analogue and digital) are connected to the external connector (X1-SIG1/K2) for supplying external systems (i.e. current sensor).

On the Logic Board v1.2 the power-on sequence for the supply signals will be following (see **Figure 62**): after applying the main power supply for the system (+12V) the IC U13 will be switched-on. As soon as VANA50/VDIG50 (VOUT of IC U13) reaches the correct level the signal RO will activate IC U14 and VDIG15 will be generated. After that the $\overline{\text{RESET}}$ output of IC U14 will turn-on IC U12 (VDIG33/VANA33). Finally the signal POWERrstn ($\overline{\text{RESET}}$ output of IC U12) will be activated waking-up the microcontroller.

For the Logic Board v1.3b is used Infineon Technologies TLE7368E Micro Controller Power Supply IC. After applying the main power supply the IC13 will be switched-on (**Figure 63**). As soon as 5V/3.3V/1.5V power supplies reached their correct values the signal POWERrstn (RO_1 and RO_2 outputs of IC12) will be activated waking-up the microcontroller.

4.4 Microcontroller

The microcontroller block (uC block overview is given in **Figure 71** for Logic Board v1.2 and in **Figure 72** for Logic Board v1.3b) contains following elements:

- TC1767 (Logic Board v1.2 on **Figure 75** and Logic Board v1.3b on **Figure 76**) is a 32-Bit Microcontroller member of the Infineon Technologies AUDO FUTURE product family designed for automotive applications. TriCore™ CPU providing high-end microcontroller performance combined with sophisticated DSP capabilities (please refer to datasheet for further details);
- Input filter (see **Figure 73** for Logic Board v1.2 and **Figure 74** for Logic Board v1.3b): passive filters for digital and analogue signals and voltage dividers for voltage level adaptation;
- EEPROM (**Figure 77**): 256kB Electrically-Erasable Programmable Read-Only Memory optimized for use in automotive applications where low-power and low-voltage operations are essential (for more details refer to AT25256A-10TQ-2.7 datasheet). The communication with the microcontroller is done through SSC0 interface (high-speed synchronous serial interface, SPI-compatible);
- RS-232 (pins ASC_TX and ASC_RX on connector X1-SIG1/K2) & CAN (pins CAN1_H and CAN1_L on connector X1-SIG1/K2) Transceivers (see **Figure 71** for Logic Board v1.2 and **Figure 72** for Logic Board v1.3b);
- Possibility to connect debugging systems like Lauterbach to the JTAG connector K3-OCDS (Header 8X2) - please refer to **Figure 64**;

4.4.1 Configuration of TC1767

The TC1767 can be configured with the respect to the different boot modes and with the respect to the different interfaces (serial/parallel) to the resolver and iGMR position sensors.

4.4.1.1 Boot Configuration of TC1767

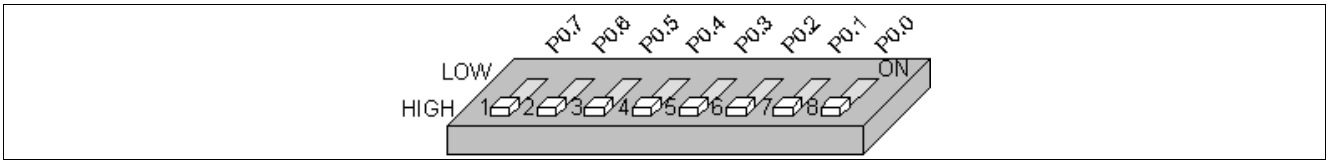


Figure 53 HW Boot Configuration of TC1767 DIP-Switch

The picture above (**Figure 53**) shows the definition of the boot HW configuration switch (DIP-Switch SW1 on **Figure 76**). The meaning of the switches will be described in the following **Table 6**.

The ON position of the switch is equal to a logical LOW at the dedicated pin.

Table 6 User Startup Modes for TC1767

CFG[7...0]	Type of Boot TC1767	1[1]	2	3	4	5	6	7	8
11XXX10X[2]	Internal Start from Flash	OFF	OFF	X[3]	X	X	OFF	ON	X
010XX100	Bootstrap Loader Mode, Generic Bootloader at CAN pins	ON	OFF	ON	X	X	OFF	ON	ON
10101100	Bootstrap Loader Mode, ASC Bootloader	OFF	ON	OFF	ON	OFF	OFF	ON	ON
10100100	Alternate Boot Mode, ASC Bootloader on fail	OFF	ON	OFF	ON	ON	OFF	ON	ON
1011X10X	Alternate Boot Mode, Generic Bootloader at CAN pins on fail	OFF	ON	OFF	OFF	X	OFF	ON	X
all others	reserved; don't use this combination								

1) 1 to 8 are the DIP-Switch numbers (SW1 on Figure 54)

2) The shadowed line indicates the default settings.

3) 'x' represents the don't care state.

4.4.1.2 Selecting Serial/Parallel Interface

DIP-4 switch (SW2 on Figure 72) is used to select serial/parallel interface for the communication with resolver or iGMR position sensor - please refer to Table 7.

Table 7 Selecting Serial/Parallel Interface

SW2[4...1]	Inetrface to the Resolver/iGMR	4[1]	3	2	1
0000[2]	iGMR enabled (SPI and Incremental mode) Resolver in Parallel Mode	OFF[3]	OFF	OFF	OFF
1111	Resolver in Serial Mode iGMR disabled	ON	ON	ON	ON
all others	reserved; don't use this combination				

1) 1 to 4 are the DIP-Switch numbers

2) 0 is equal to open switch, "1" is equal to closed switch

3) 'x' represents the don't care state.

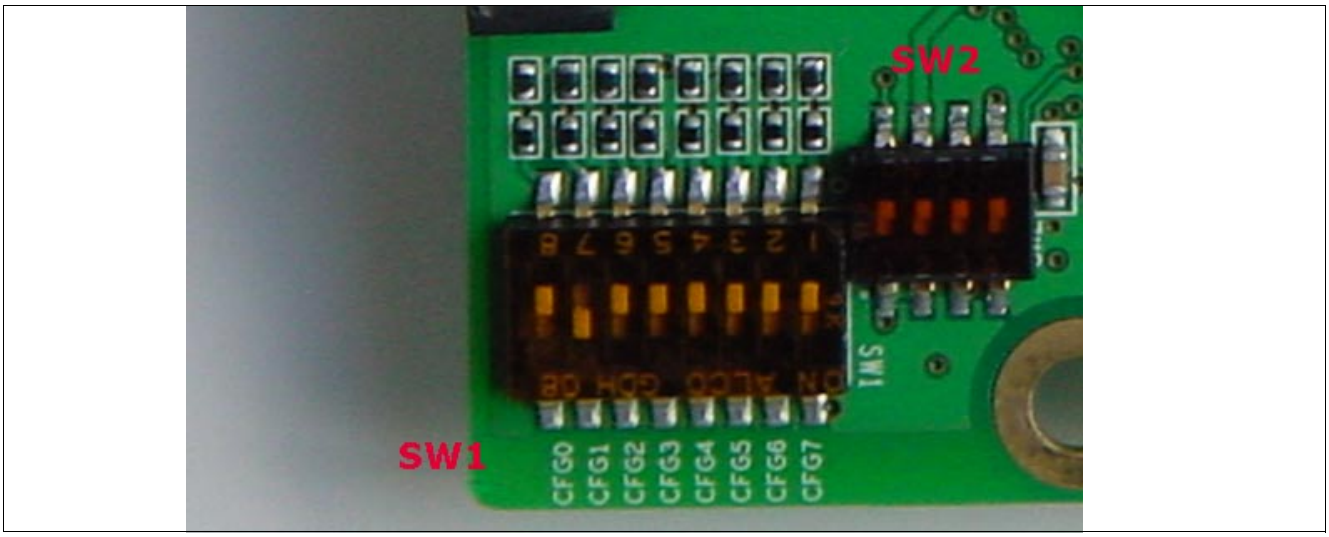


Figure 54 The Boot Configuration Switch (SW1) and Serial/Parallel Interface Select Switch (SW2)

4.5 Watchdog

The Logic Board contains a pin-selectable watchdog timer that supervises the microcontroller activity and signalizes when the system is operating improperly. During normal operation, the microcontroller (GPTA39) should repeatedly toggle the watchdog input (WDI, see **Figure 65**) before the selected watchdog time-out period elapses to report that the system is processing code properly. If this does not occurs, the supervisor asserts a watchdog output ($\overline{WDO}$) which will reset the microcontroller via PORSTn (external power-on hardware reset).

The state of the three logic control pins (SET0, SET1 and SET2) determines watchdog timing characteristics (see table in **Figure 65**). The jumper J1 allows disabling the watchdog functionality in a very easy way.

4.6 Phase Current Sensing

Phase current sensing signals should be connected to the Logic Board connector X1-SIG1/K2 to the pins I_U, I_V and I_W (**Figure 73** for the Logic Board v1.2 and **Figure 74** for the Logic Board v1.3b). The Logic Board is designed to work with current transducers (not provided with the Hybrid Kit) with voltage output proportional to the current (usually deploying Hall effect - like LEM sensors). User can take +5V (analog) available on the X1-SIG1/K2 pins to supply current transducers. The exact type of current transducer will be depend on many parameters in application, but usually the most important is the motor current consumption. Please notice that if you control 3-phase balanced synchronous system it is enough to measure just 2 phases, since the 3rd phase current can be calculated as algebraic combination out of the 2 measured currents.

4.7 Resolver Interface

The Logic Board includes a 12-Bit Resolver-to-digital converter (meaning A/D converter) which integrates an on-board programmable sinusoidal oscillator that provides sine wave excitation for resolvers (pins R1 and R2 on connector X1-SIG1/K2). For more details please refer to the data sheet of the component (AD2S1200YST) and the schematics of the circuit - for Logic Board v1.2 see **Figure 66** and for Logic Board v1.3b see **Figure 67**. With resistors (R155, R156, R157, R158, R159 and R160) user can trim the LMH6672 (dual op-amp) output voltage values (resolver excitation). On the Logic Board v1.3b is given additional possibility to trim the resolver excitation with potentiometers (R483, R484, R485 - not populated, user should solder them if needed). Please refer to data sheet of used resolver to trim this values properly. The resolver response should be connected between pins S1 and S3 (sine) and S2 and S6 (cosine) on the connector X1-SIG1/K2.

4.8 Encoder Interface

If encoder is used as a sensor for the motor position/speed sensing the following pins on connector X1-SIG1/K2 should be connected: the phase A should be connected to pin PosA (Logic Board v1.2) or between pins PosA/iGMR_A+ and PosA/iGMR_A- (Logic Board v1.3), the phase B should be connected to pin PosB (Logic Board v1.2) or between pins PosB/iGMR_B+ and PosB/iGMR_B- (Logic Board v1.3b) and phase Z (index or zero marker) should be connected to pin PosZ (Logic Board v1.2) or between pins PosZ/iGMR_Z+ and PosZ/iGMR_Z- (Logic Board v1.3b).

4.9 Hall Sensor Interface

If Hall sensor is used as a sensor for the motor position/speed sensing the following pins on connector X1-SIG1/K2 should be connected: the phase U should be connected to pin PosU (Logic Board v1.2) or to pin PosU/iGMR_U (Logic Board v1.3b), the phase V should be connected to pin PosV (Logic Board v1.2) or to pin PosV/iGMR_V (Logic Board v1.3b) and phase W should be connected to pin PosW (Logic Board v1.2) or to pin PosW/iGMR_W (Logic Board v1.3b).

4.10 GMR Interface

As mentioned on the beginning of the **Chapter 4**, the Logic Board v1.3b supports GMR interface by means of a bi-directional SSC (SPI compatible), encoder (or incremental) and Hall sensor interface. It is explicitly recommended to use Infineon Technologies TLE5012 GMR-based angular sensor for rotor position sensing. The TLE 5012 is a 360° angle sensor that detects the orientation of a magnetic field. This is achieved by measuring sine and cosine angle components with monolithic integrated Giant Magneto Resistance. For more details about TLE5012 please refer to the data sheets on Infineon Technologies internet pages.

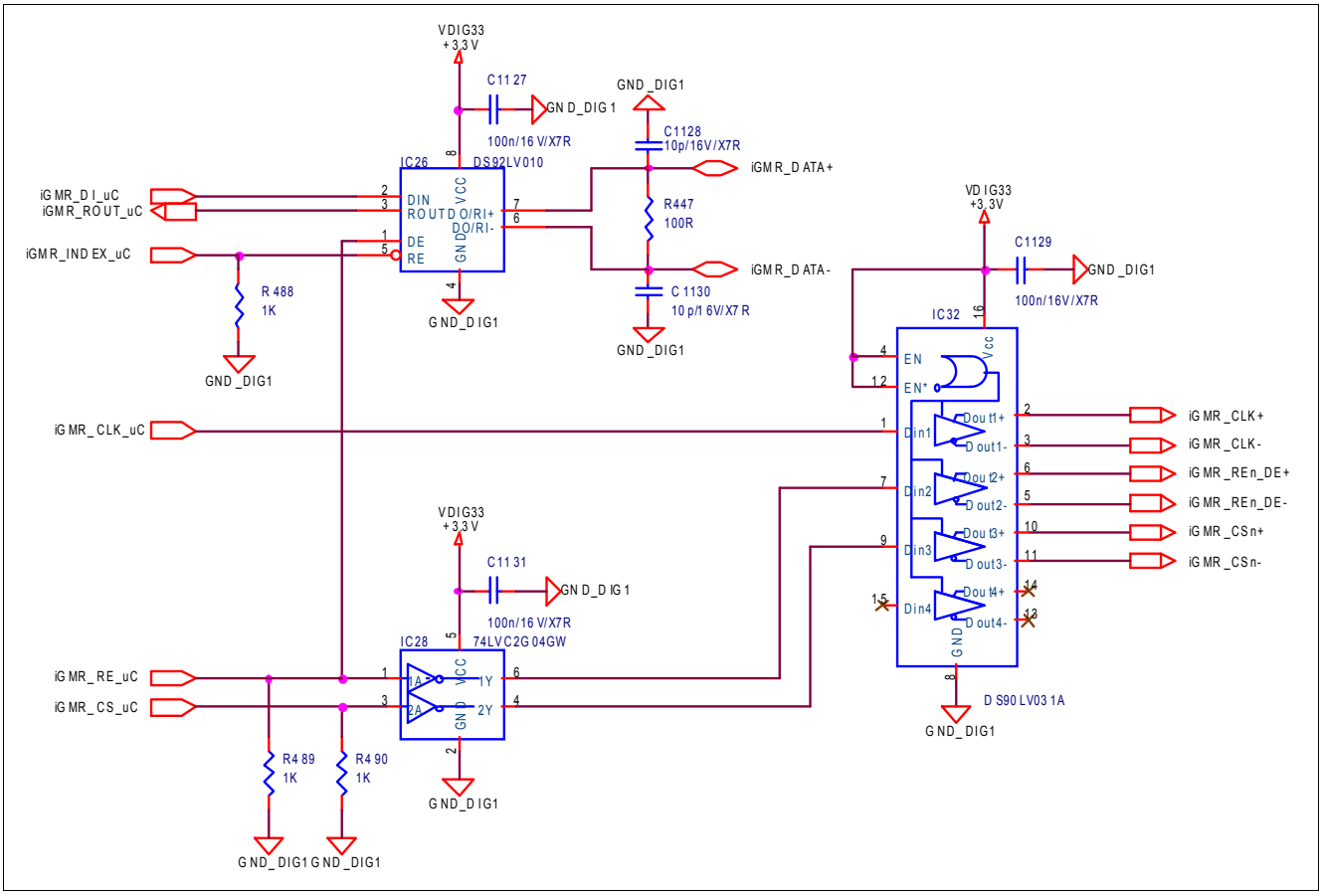


Figure 55 GMR SSC Interface (Logic Board v1.3b only)

4.10.1 GMR SSC Interface Mode

The schematics of SSC interface on the Logic Board is shown on **Figure 55**. Signals on connector X1-SIG/K2 that are used for SSC interface are: iGMR_CSn+/iGMR_CSn- (Chip Select, differential signals), iGMR_REn_DE+/iGMR_REn_DE- (Read Enable, differential signals), iGMR_DATA+/iGMR_DATA- (Serial Data, differential signals) and iGMR_CLK+/iGMR_CLK- (SSC Clock, differential signals) - all signals are listed in **Table 5**. On **Figure 56** is presented the schematics of possible technical solution (implemented by Infineon Technologies System Engineering) for usage of TLE5012. The PCB with TLE5012 and a few additional components is mounted perpendicular to the electric motor shaft - just as shown on **Figure 57**. The TLE5012 is on the opposite side of the PCB - next to the motor shaft.

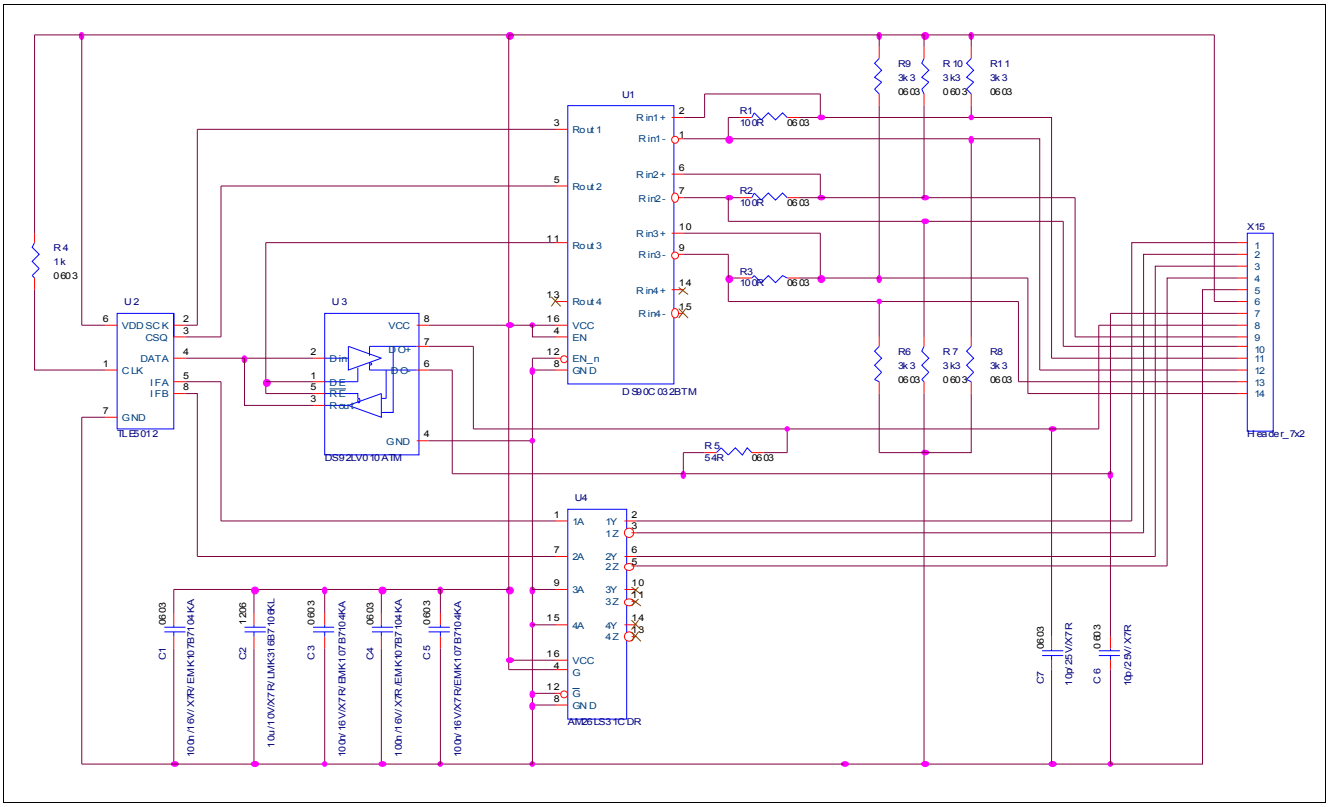


Figure 56 GMR SSC Interface - Proposal Using TLE5012

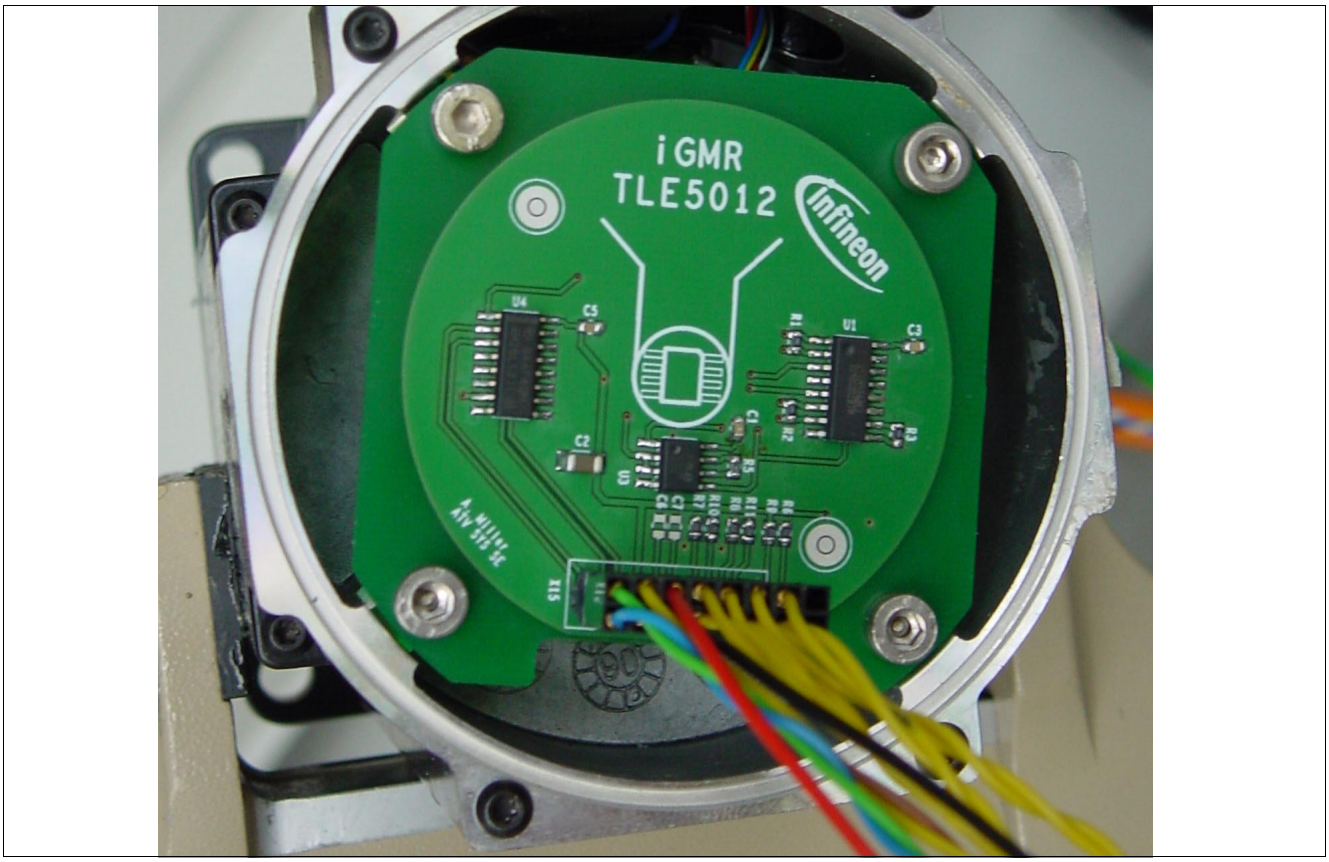


Figure 57 Picture of Possible Physical Implementation of the GMR Sensor

4.10.2 GMR Encoder Interface Mode

Infineon Technologies iGMR sensor TLE5012 can be used with encoder interface as well. This working mode is referred as IIF Interface mode in theTLE5012 data sheet. To avoid signal integrity and EMC problems, within Hybrid Kit it is expected that the 2 phase signals (A and B) and zero (index) signal are provided differentially. On the connector X1_SIG (**Figure 51**) encoder inputs are: PosA/iGMR_A+ and PosA/iGMR_A (phase A), PosB/iGMR_B+ and PosB/iGMR_B (phase B) and PosZ/iGMR_Z and PosZ/iGMR_Z (phase Z - index) - please refer to the **Table 5**. Please refer to the TLE5012 data sheet to get iGMR sensor running in incremental mode.

4.10.3 GMR Hall Sensor Interface Mode

TLE5012 supports Hall sensor interface mode as well (iGMR emulates Hall sensor mode). For this purpose to the connector X1-SIG/K2 inputs PosU/iGMR_U (phase U), PosV/iGMR_V (phase V) and PosW/iGMR_W (phase W) should be connected. Please notice (on **Figure 74**) that the pull-up resistors to 3.3V (R491, R492 and R493) are already provided on the Logic Board. For more details on Hall sensor mode please refer to the TLE5012 data sheet.

4.11 Definition of Layers for the Logic Board

The Logic Board was made keeping the following rules for the copper thickness and the space between different layers shown in **Figure 58** for the Logic Board v1.2 (4 layers) and **Figure 59** for the Logic Board v1.3b (6 layers).

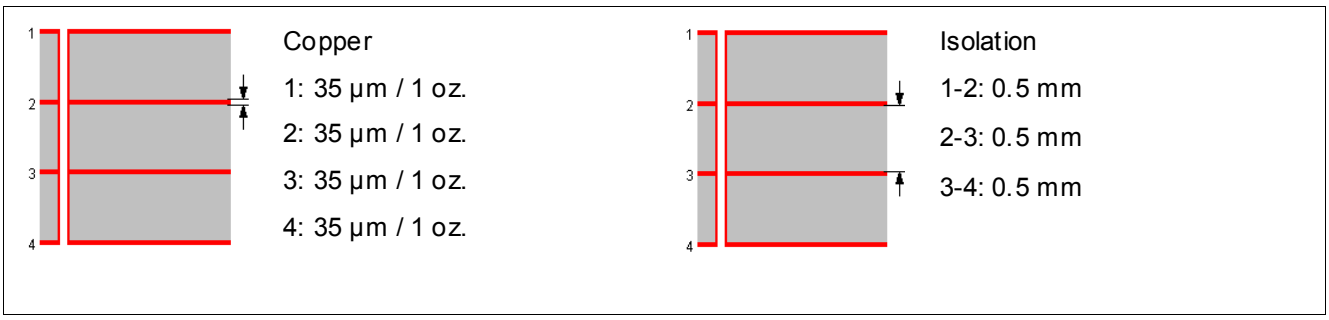


Figure 58 Definition of the Layers for the Logic Board v1.2

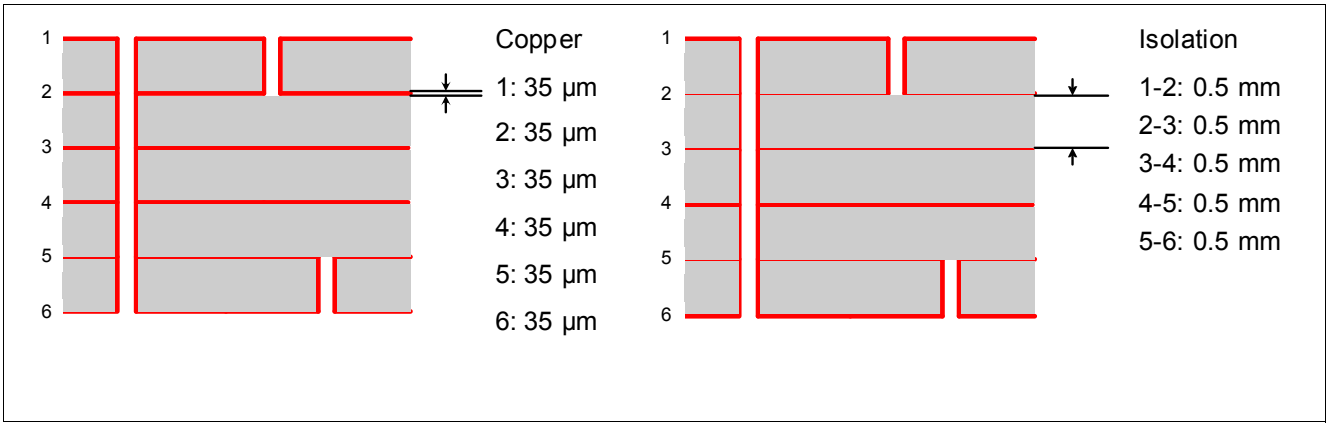


Figure 59 Definition of the Layers for the Logic Board v1.3b

4.12 Schematics, Layout and Bill of Materials

To meet the individual customer requirements and to make the Logic Board for the HybridPACK™2 module as a platform for development or modifications, all necessary technical data like schematics, layout and components for the Logic Board are included in this chapter.

4.12.1 Schematics

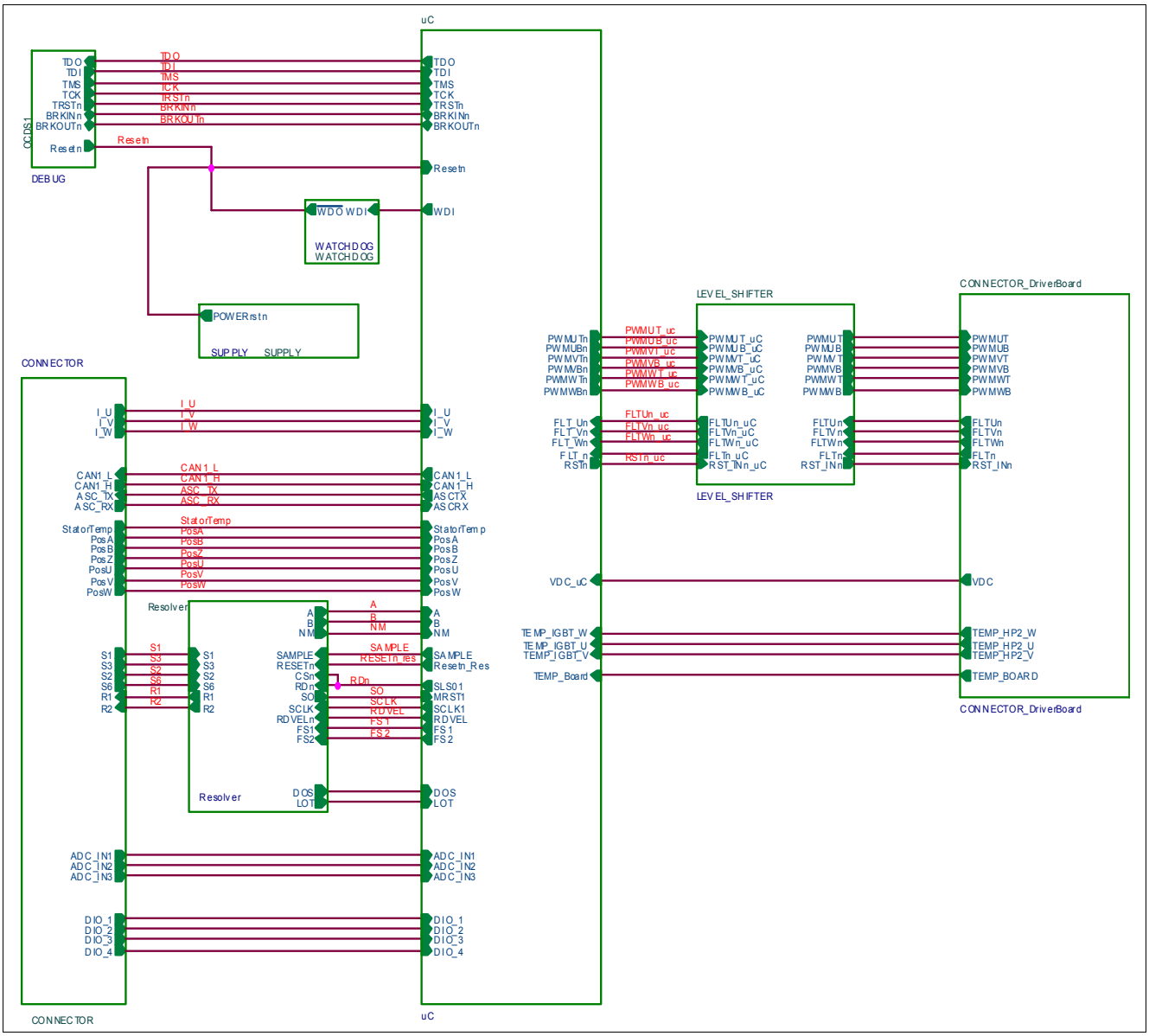


Figure 60 Schematics Block Overview Logic Board v1.2

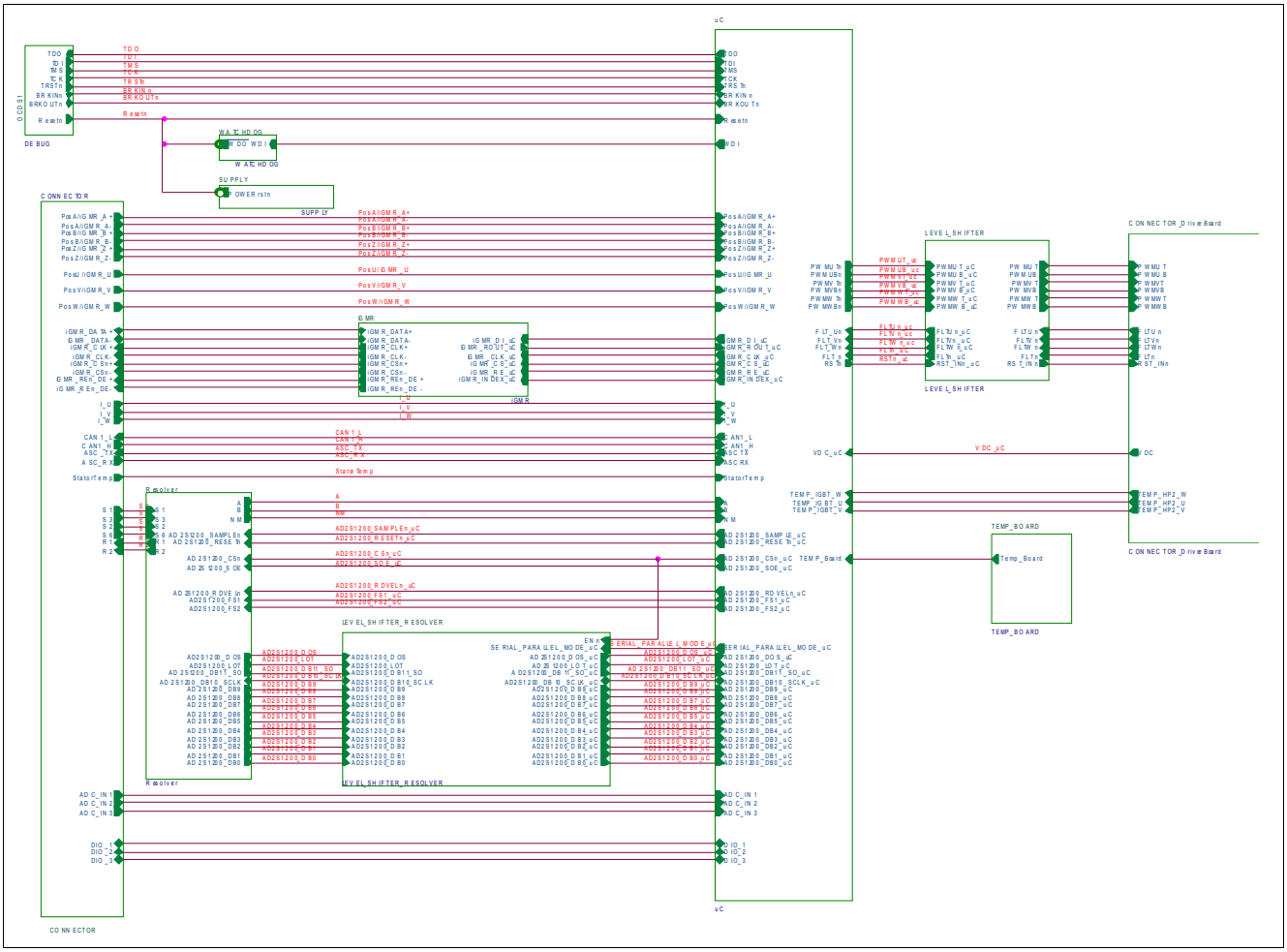


Figure 61 Schematics Block Overview Logic Board v1.3b

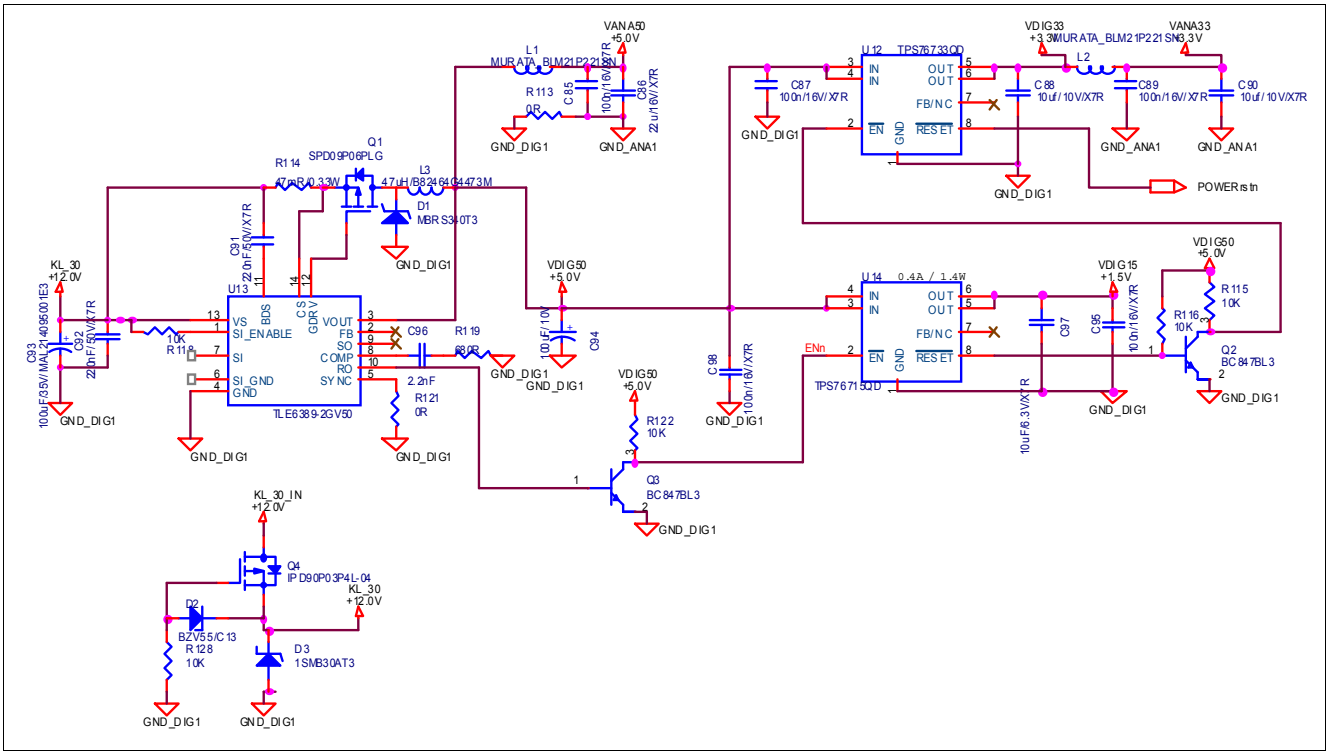


Figure 62 Power Supply Logic Board v1.2

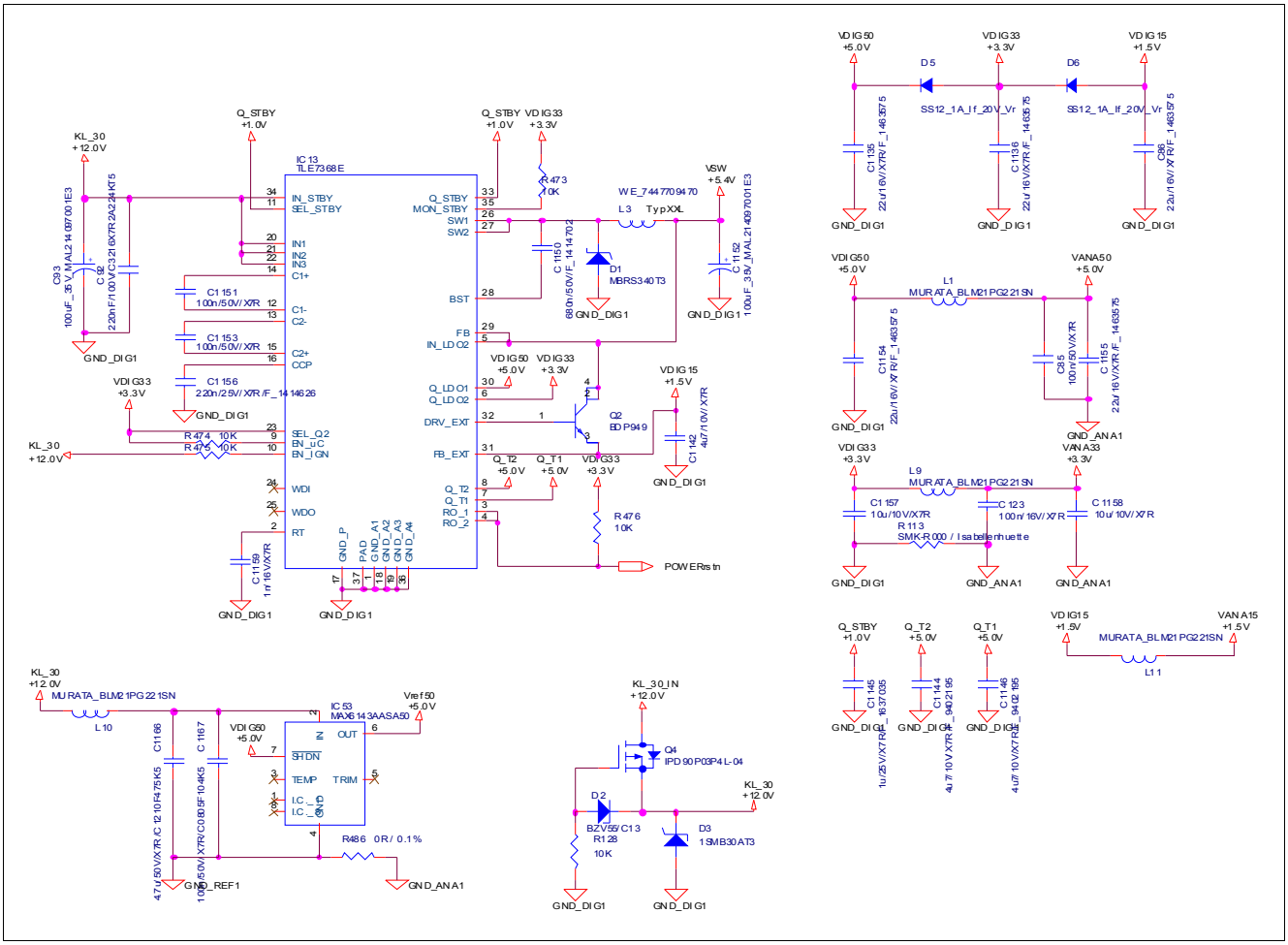


Figure 63 Power Supply Logic Board v1.3b

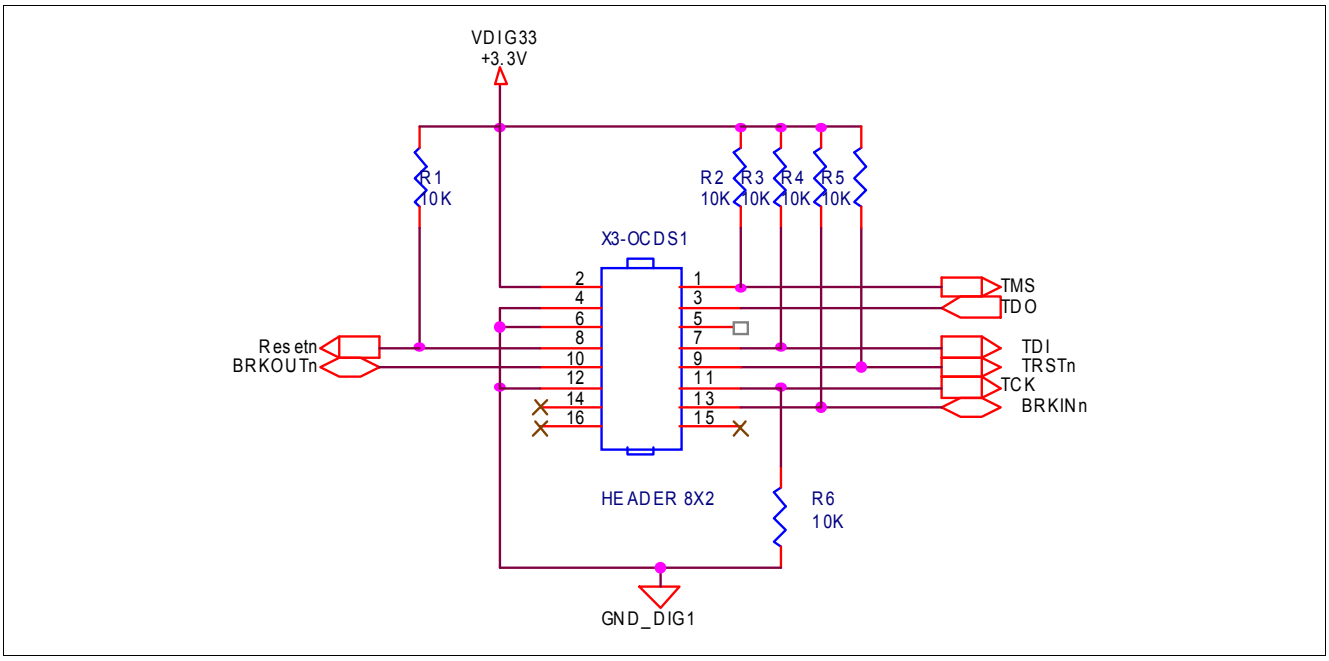


Figure 64 JTAG Debug Connector (same for Logic Board v1.2 and v1.3b)

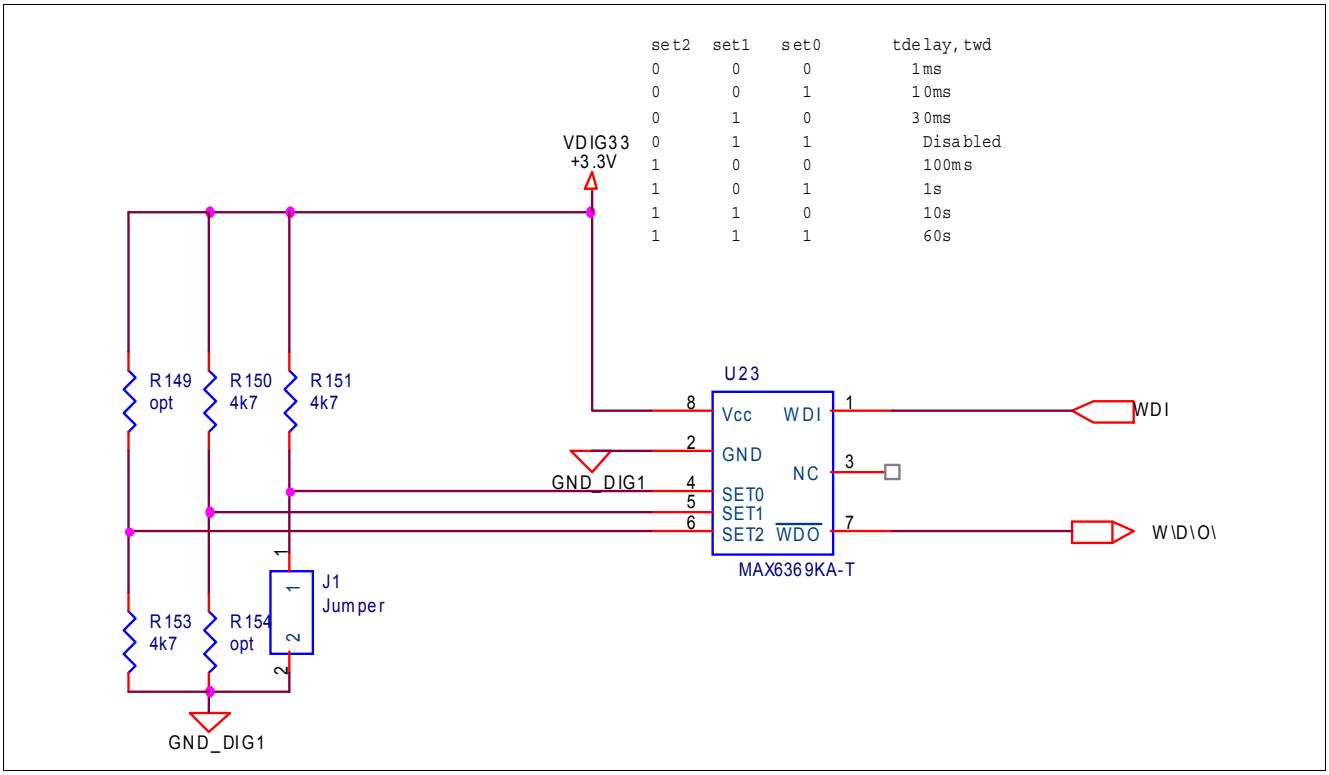


Figure 65 Watchdog (same for Logic Board v1.2 and v1.3b)

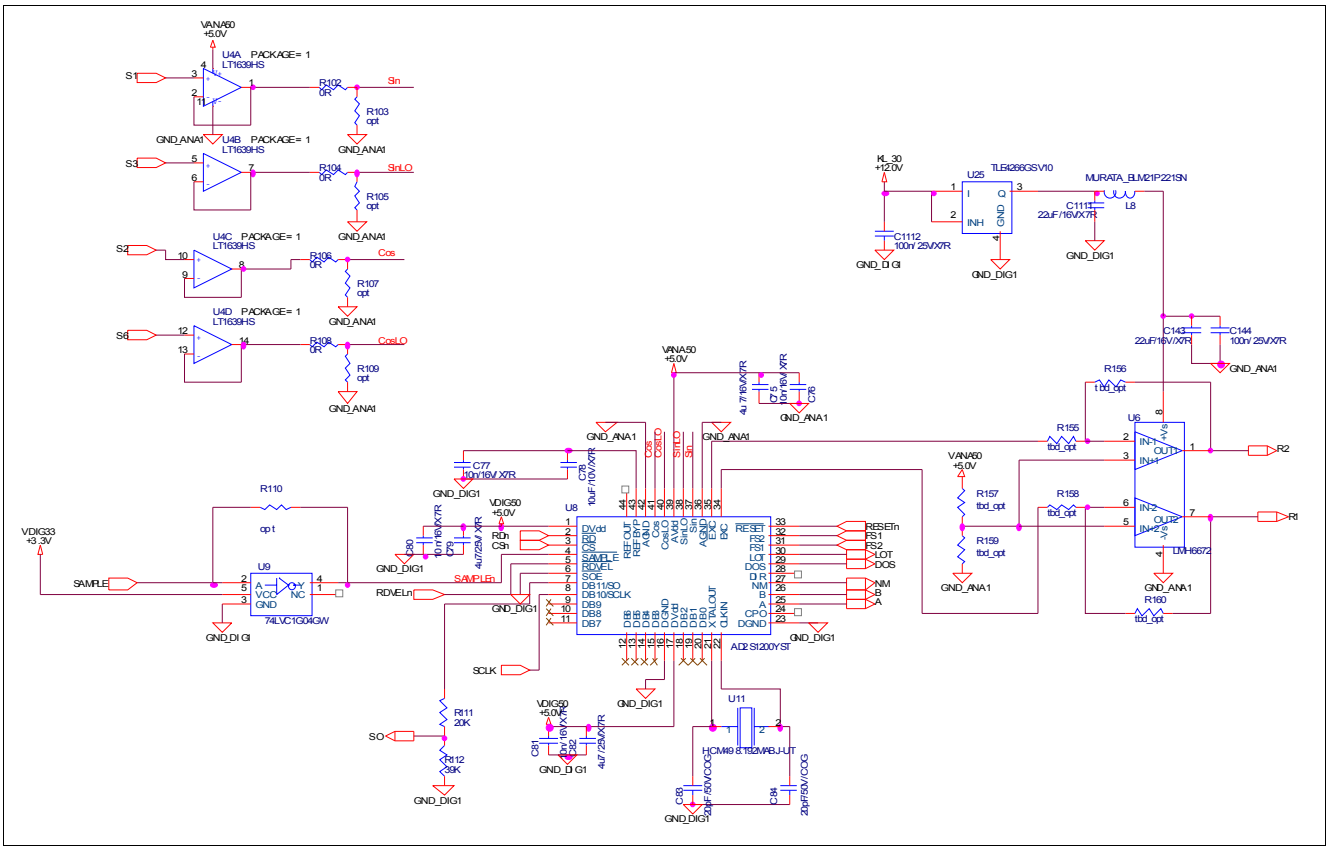


Figure 66 Resolver Logic Board v1.2

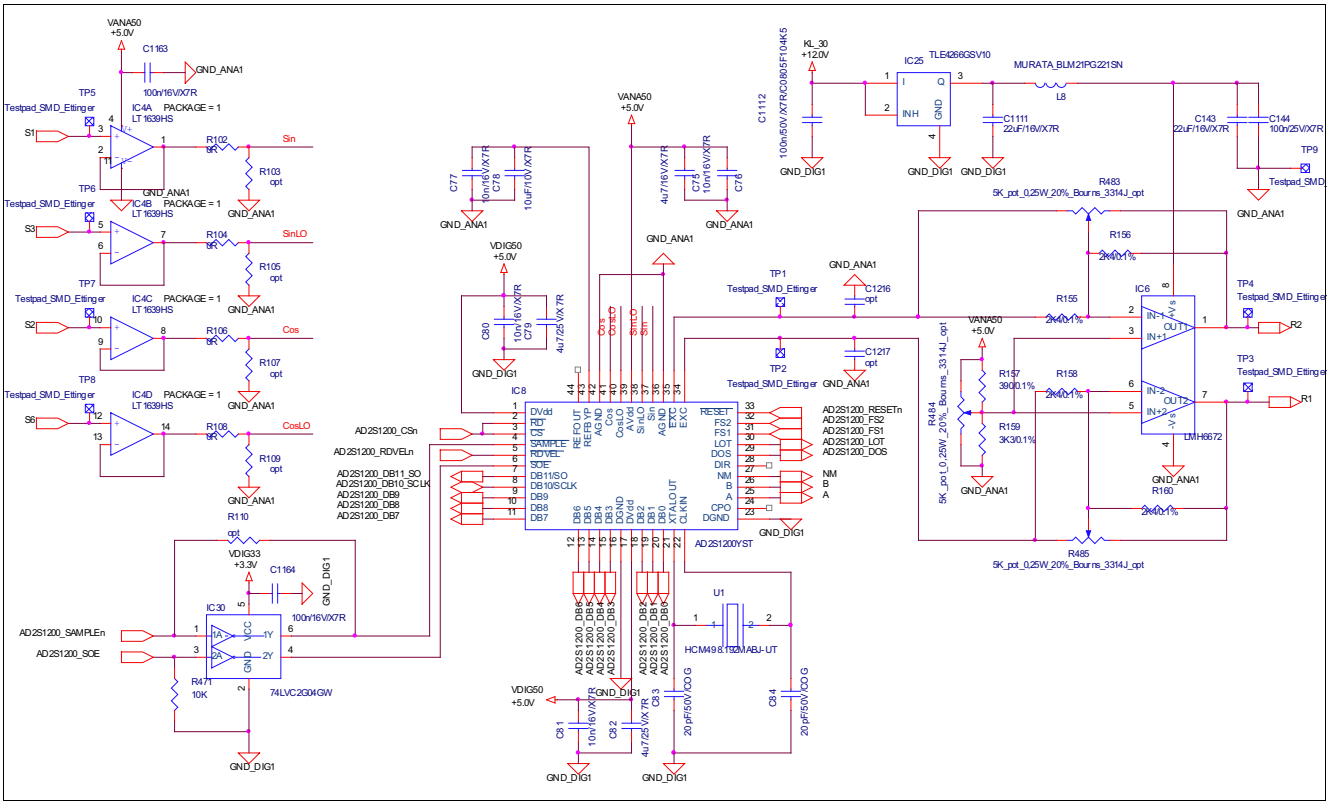


Figure 67 Resolver Logic Board v1.3b

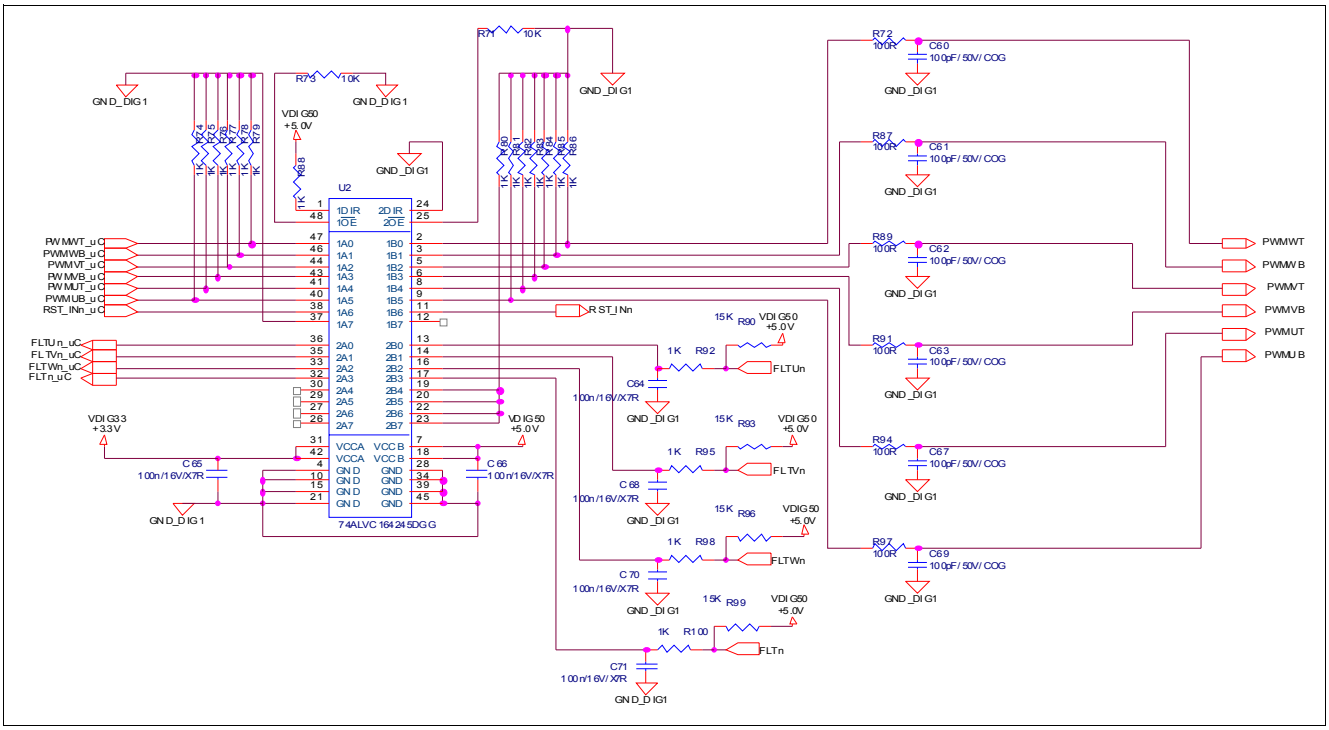


Figure 68 Level Shifter for Adapting 3.3V to 5V Logic Levels Logic Board v1.2

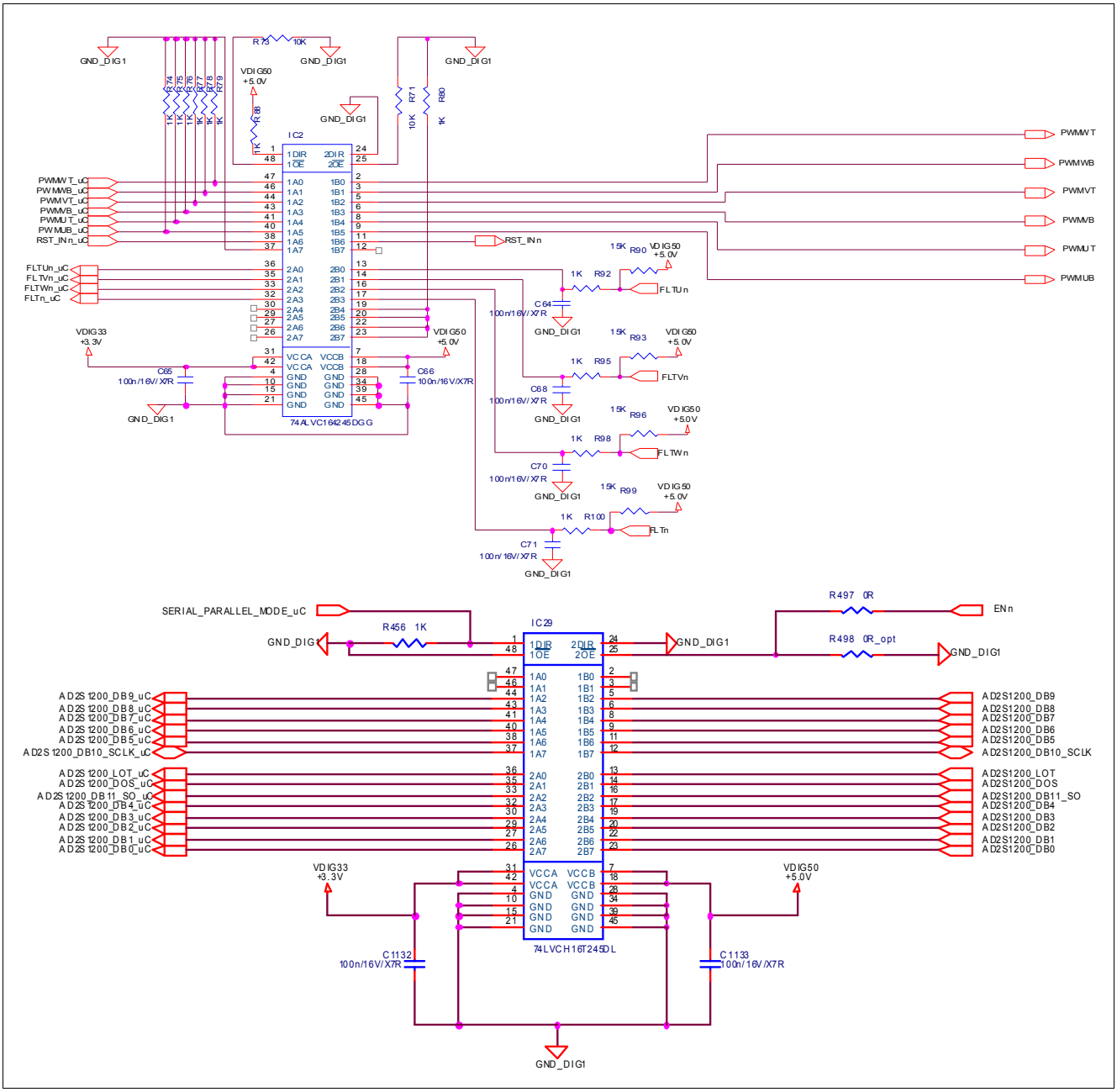


Figure 69 Level Shifter for Adapting 3.3V to 5V Logic Levels Logic Board v1.3b

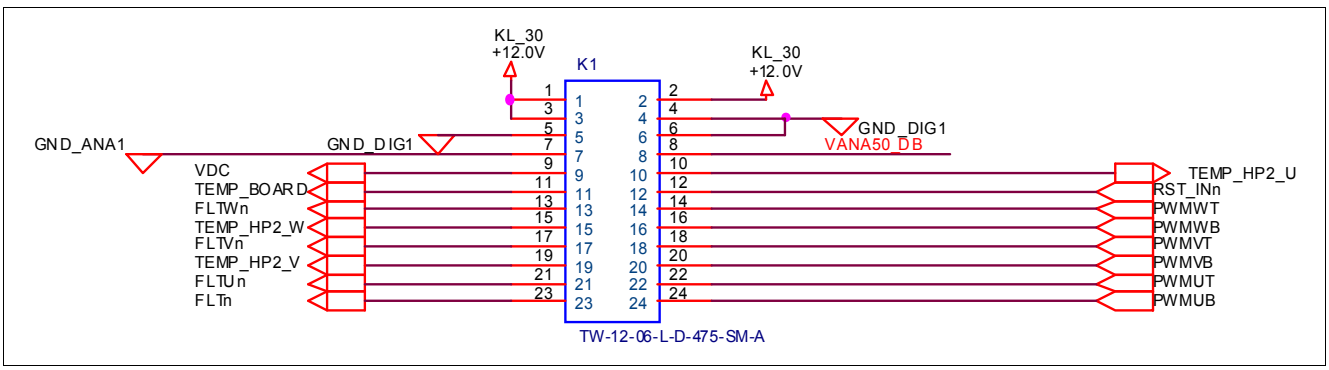


Figure 70 Connector to the Driver Board (same for Logic Board v1.2 and v1.3b)

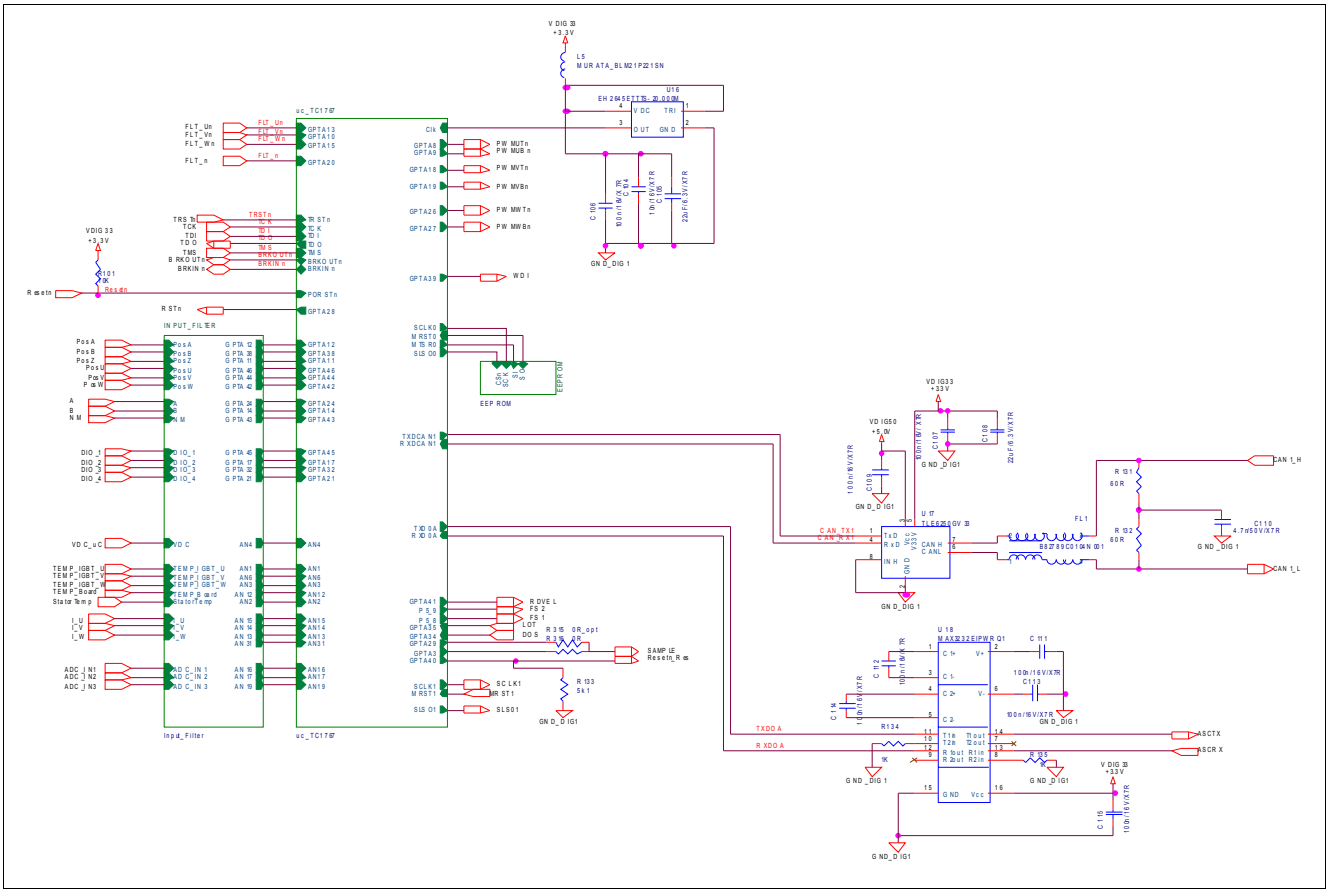


Figure 71 Microcontroller Logic Board v1.2

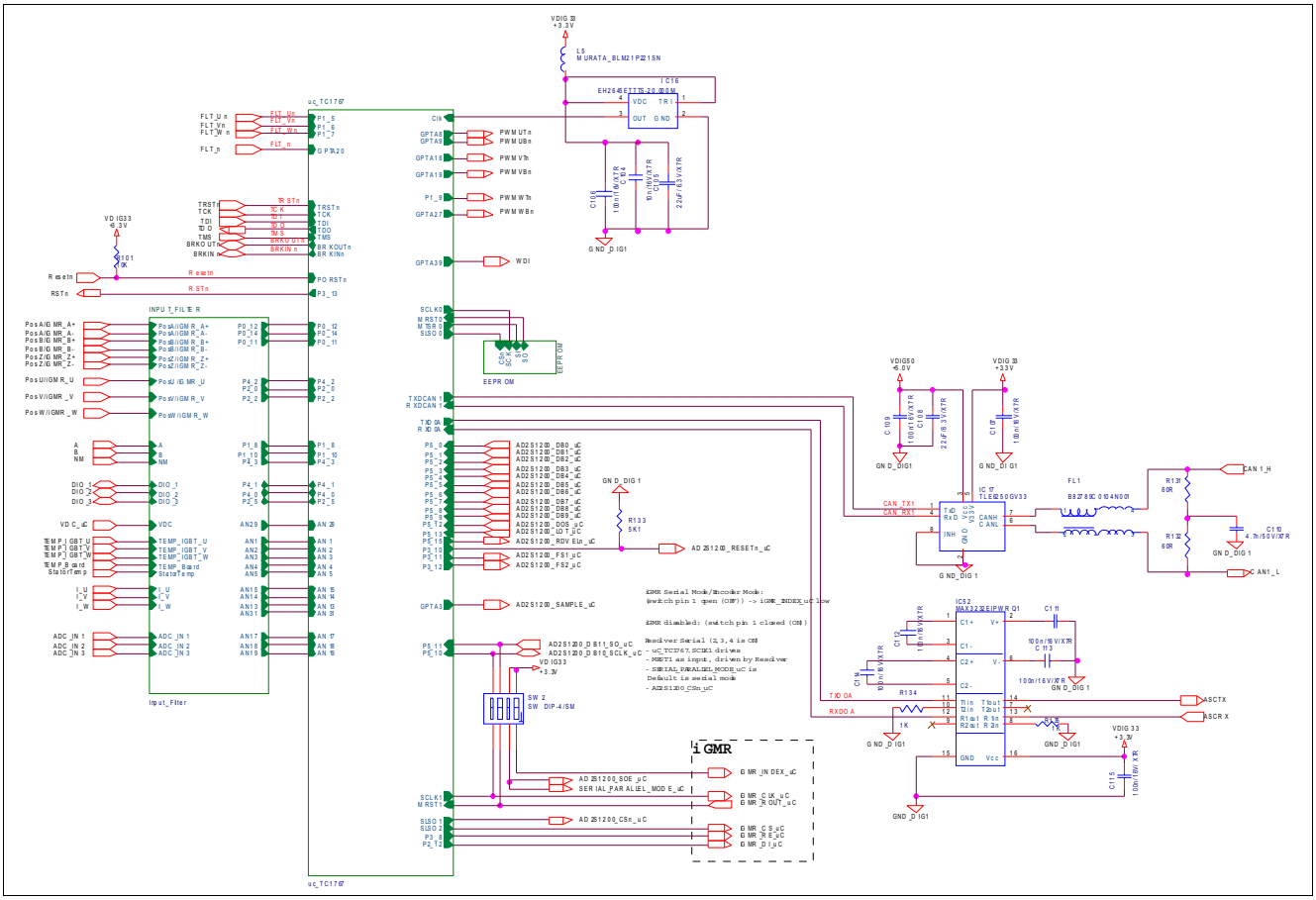


Figure 72 Microcontroller Logic Board v1.3b

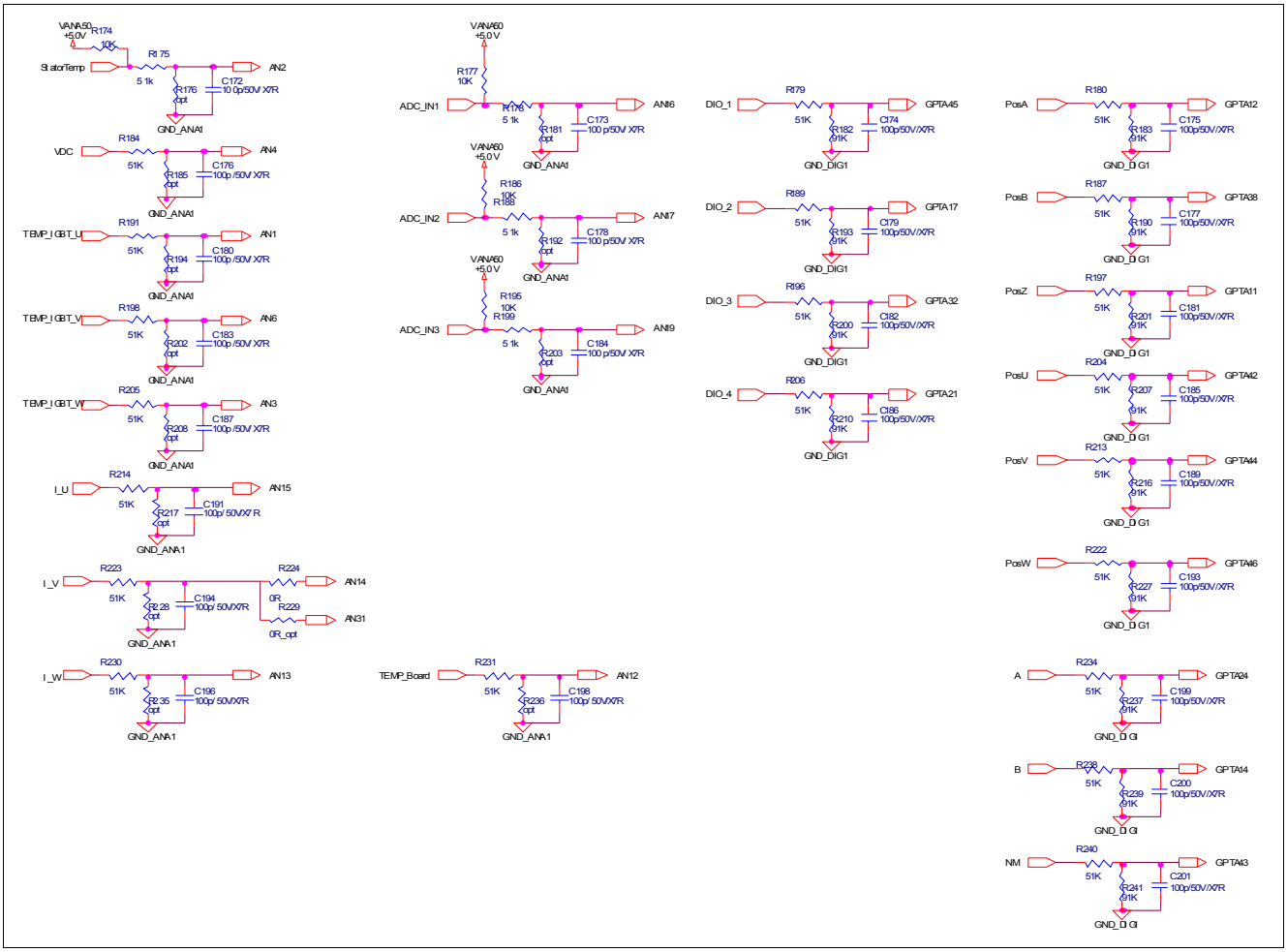


Figure 73 Input Filter Logic Board v1.2

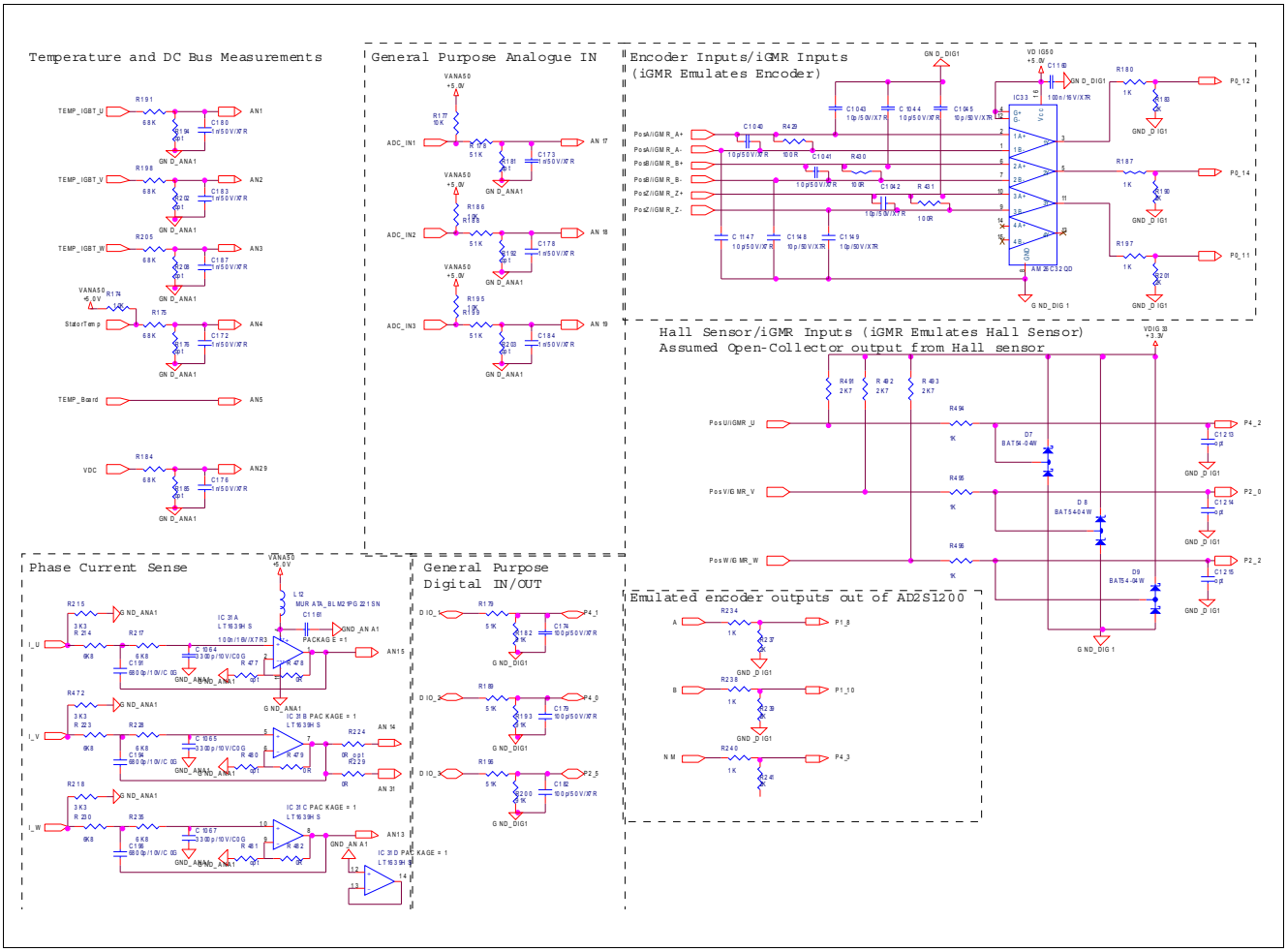


Figure 74 Input Filter Logic Board v1.3b

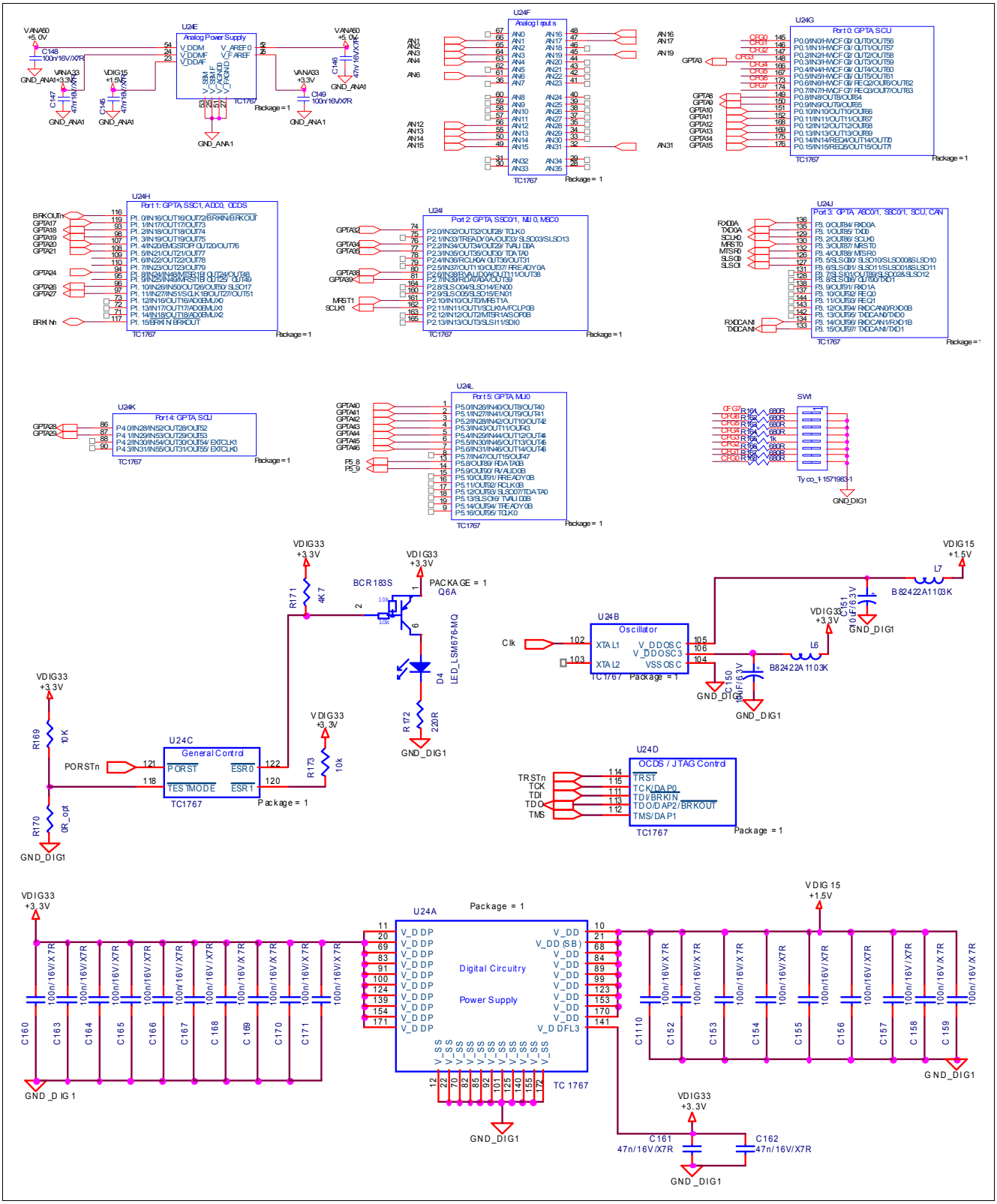


Figure 75 Microcontroller TC1767 Pin Assignment Logic Board v1.2

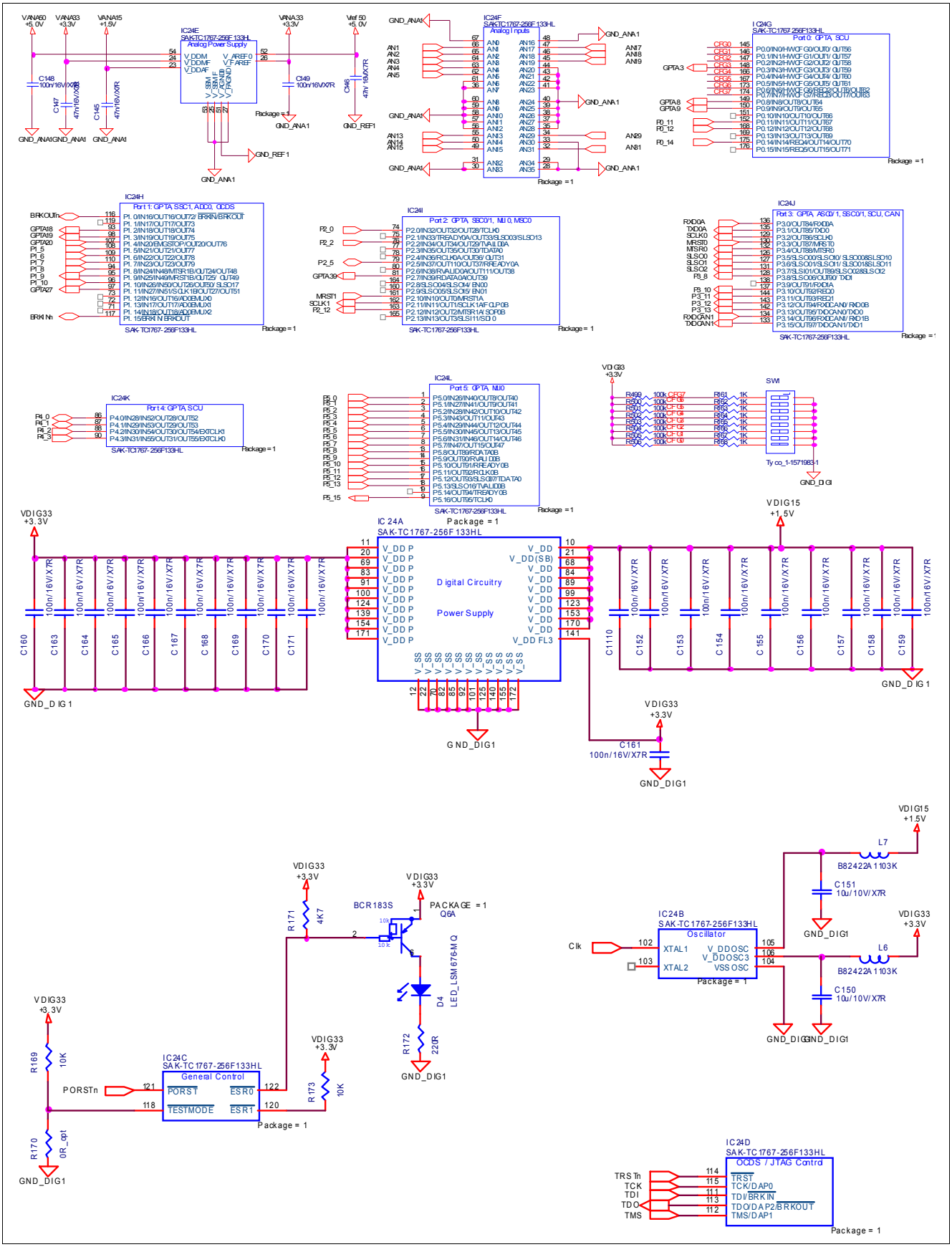


Figure 76 Microcontroller TC1767 Pin Assignment Logic Board v1.3b

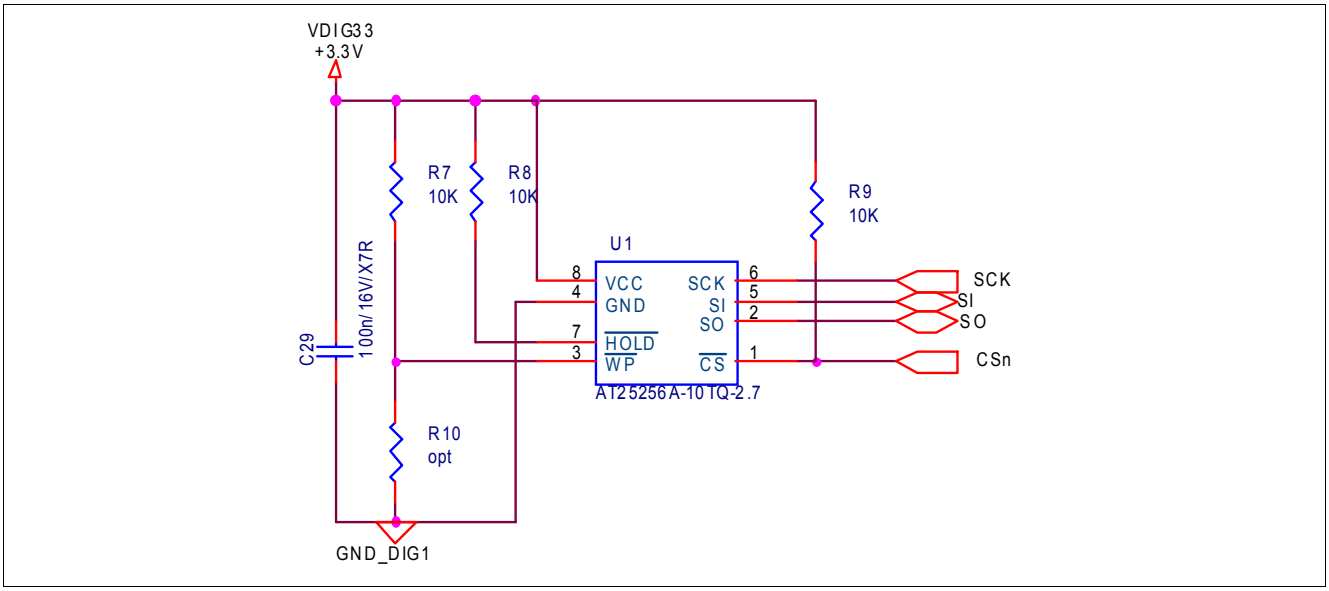


Figure 77 EEPROM (same for Logic Board v1.2 and Logic Board v1.3b)

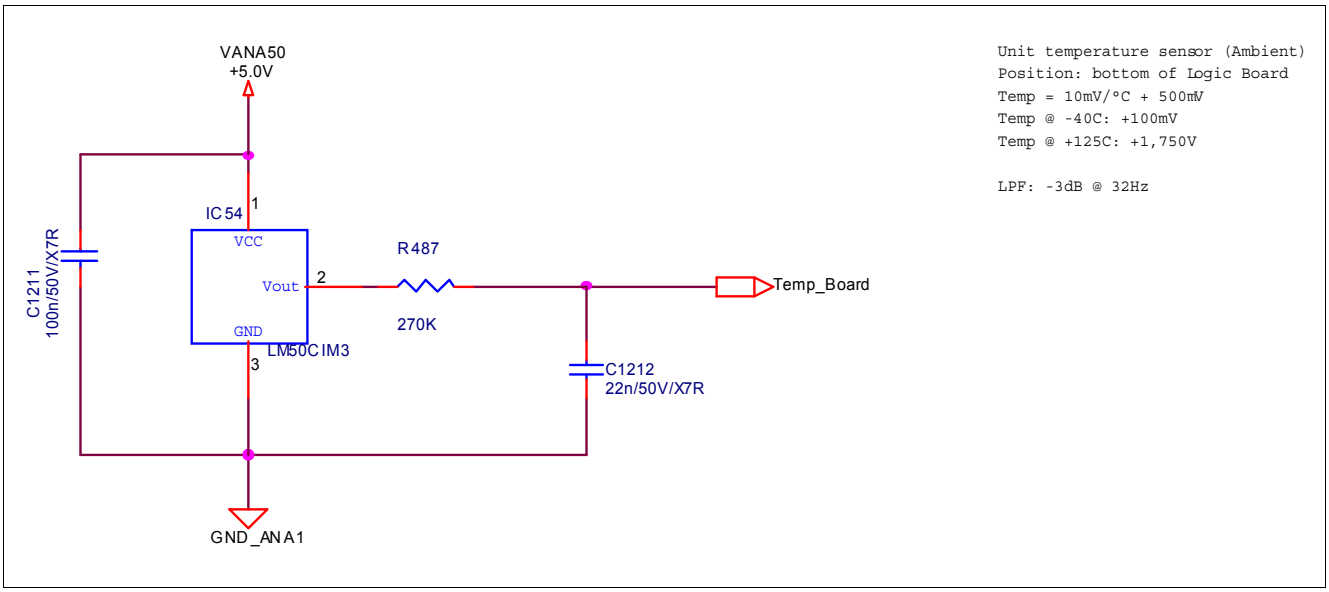


Figure 78 On-Board Temperature Measurement (Logic Board v1.3b only)

4.12.2 Assembly Drawing

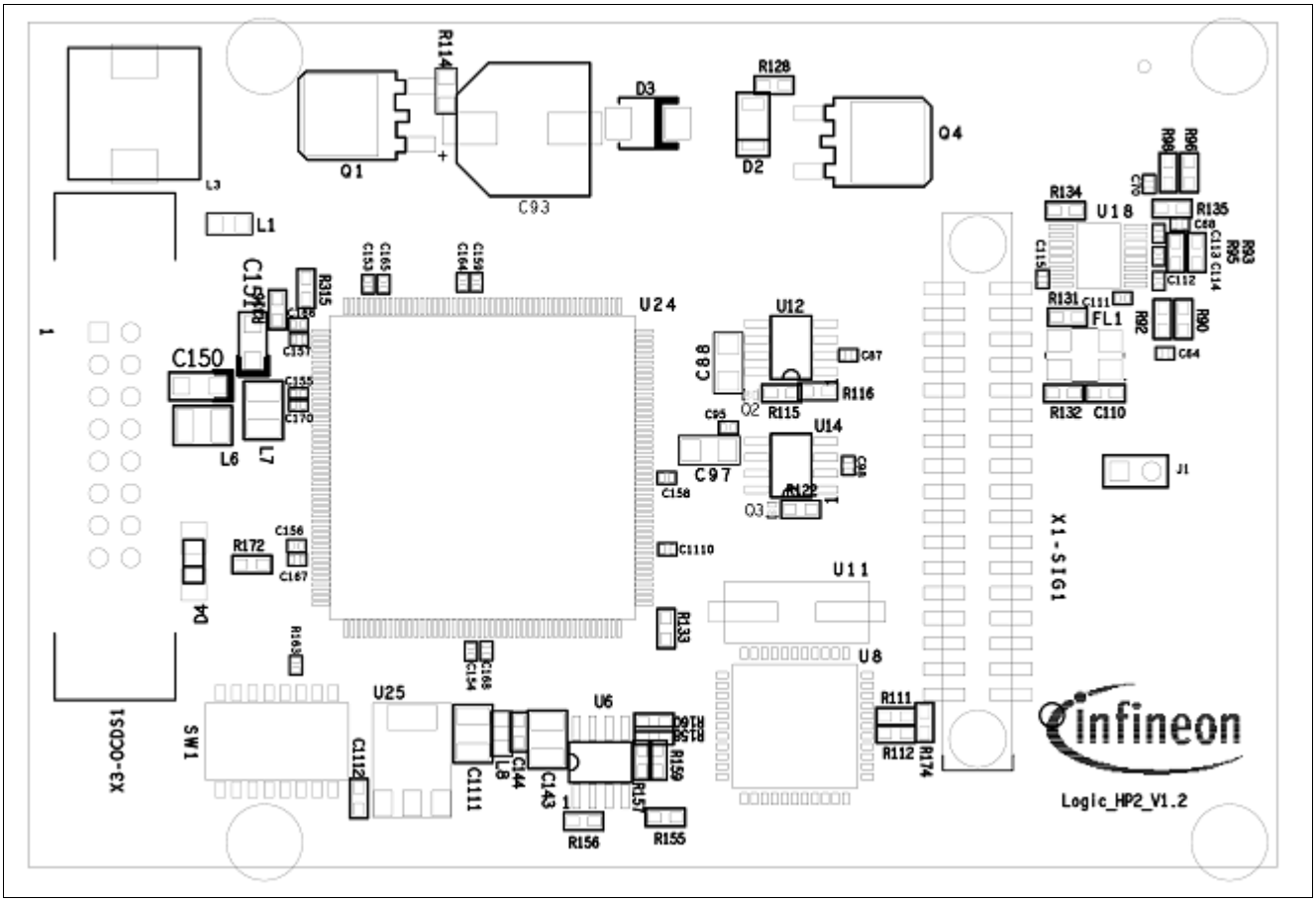


Figure 79 Assembly Drawing of the Logic Board v1.2 (Top)

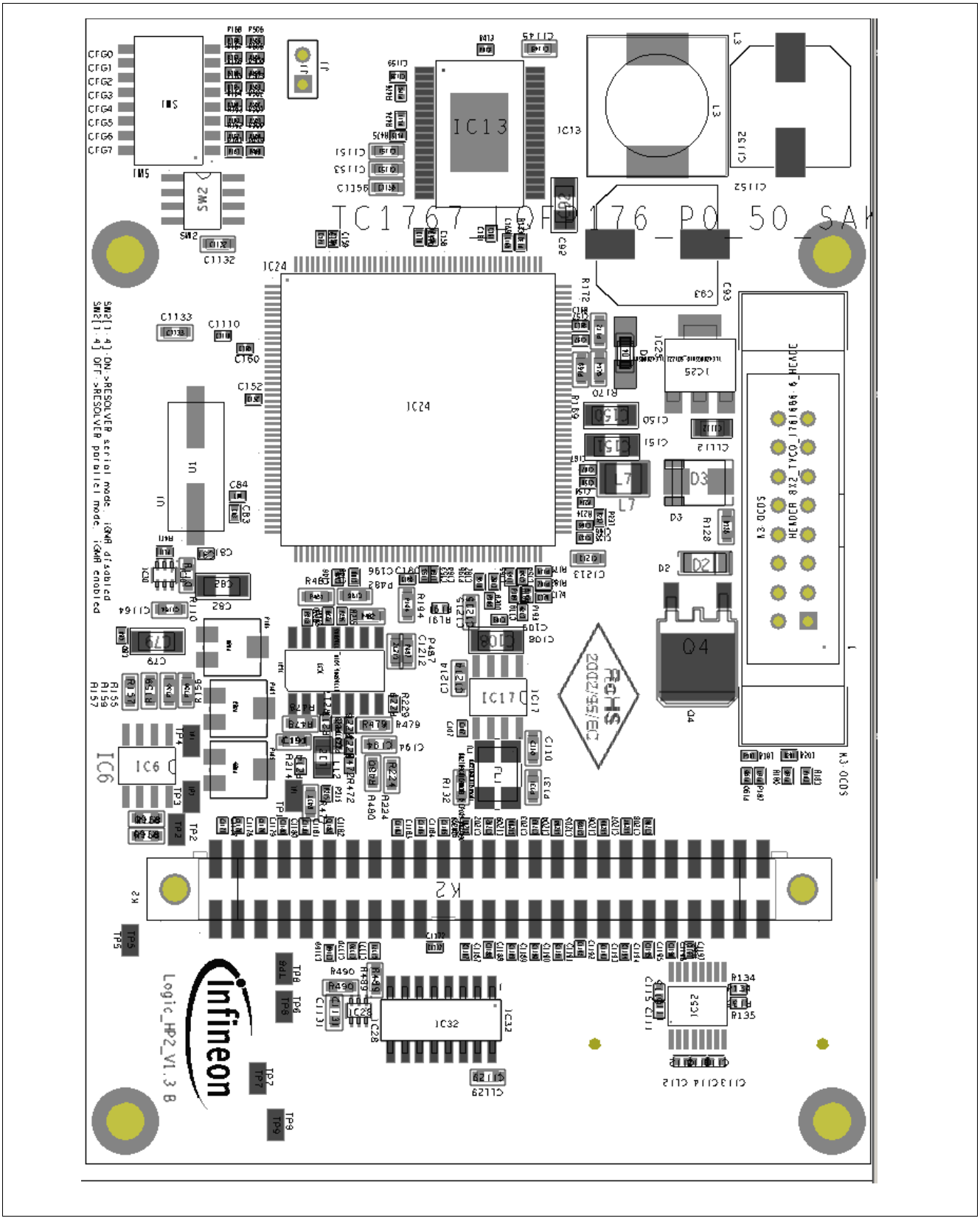


Figure 80 Assembly Drawing of the Logic Board v1.3b (Top)

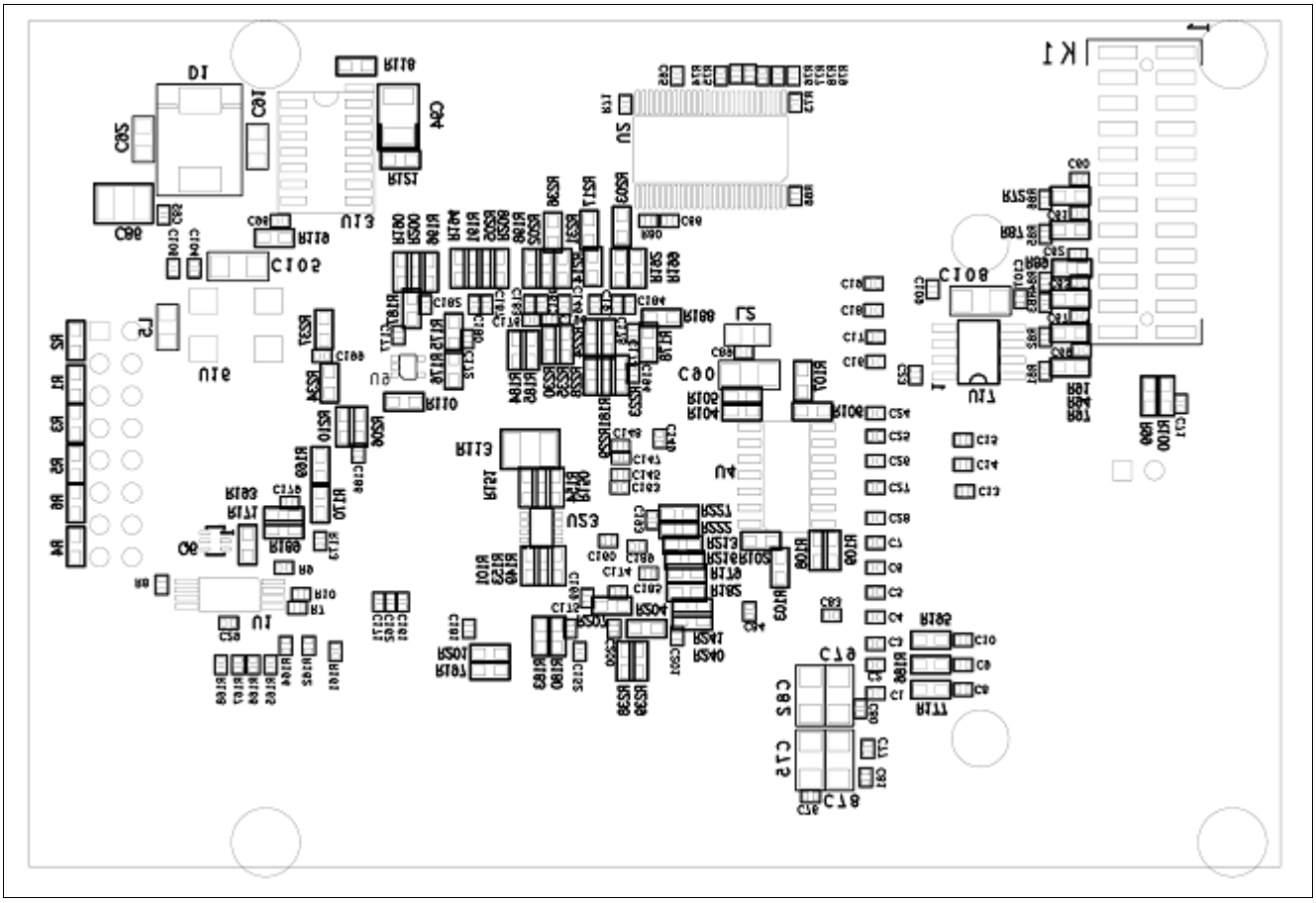


Figure 81 Assembly Drawing of the Logic Board v1.2 (Bottom)

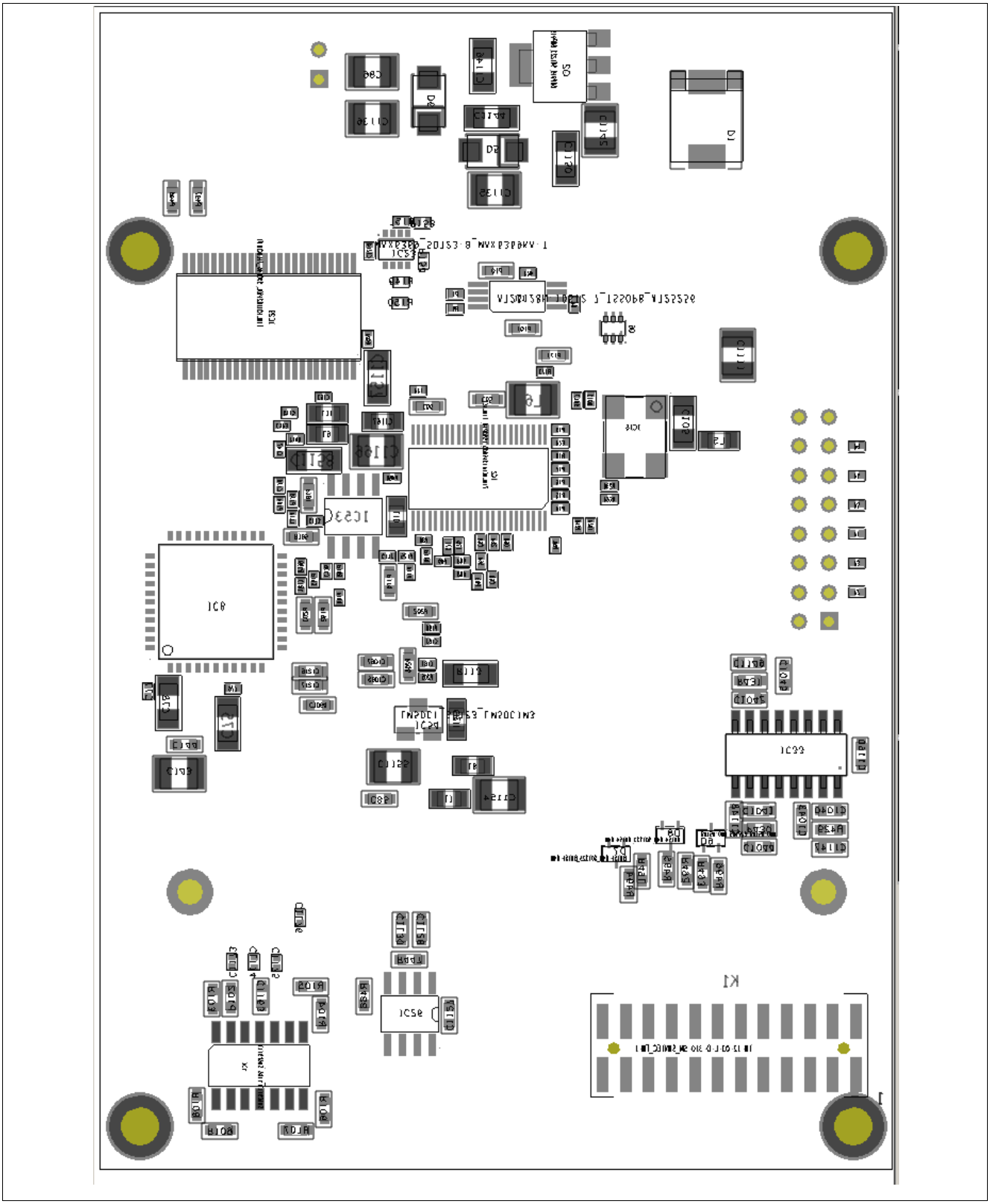


Figure 82 Assembly Drawing of the Logic Board v1.3b (Bottom)

For detail information use the zoom function of your PDF viewer to zoom into the drawings on **Figure 79**, **Figure 80**, **Figure 81** and **Figure 82**.

4.12.3 Layout

Layout of the Logic Board v1.2 is shown on **Figure 83** (Top Layer), on **Figure 84** (Layer 2), on **Figure 85** (Layer 3) and on **Figure 86** (Bottom Layer).

Layout of the Logic Board v1.3b is shown on **Figure 87** (Top Layer), on **Figure 88** (Layer 2), on **Figure 89** (Layer 3), on **Figure 90** (Layer 4), on **Figure 91** (Layer 5) and on **Figure 92** (Bottom Layer).

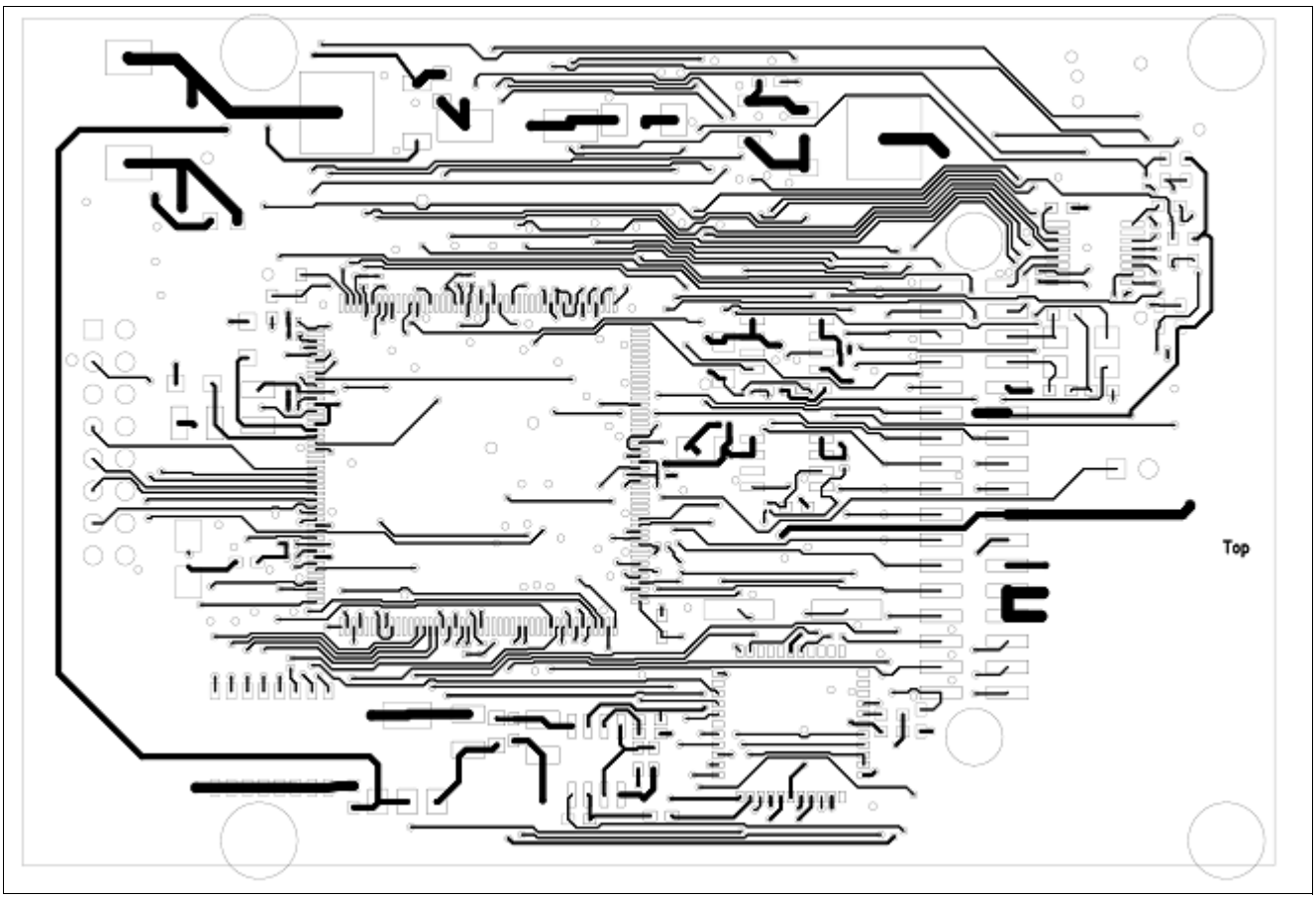


Figure 83 Logic Board v1.2 - Top Layer

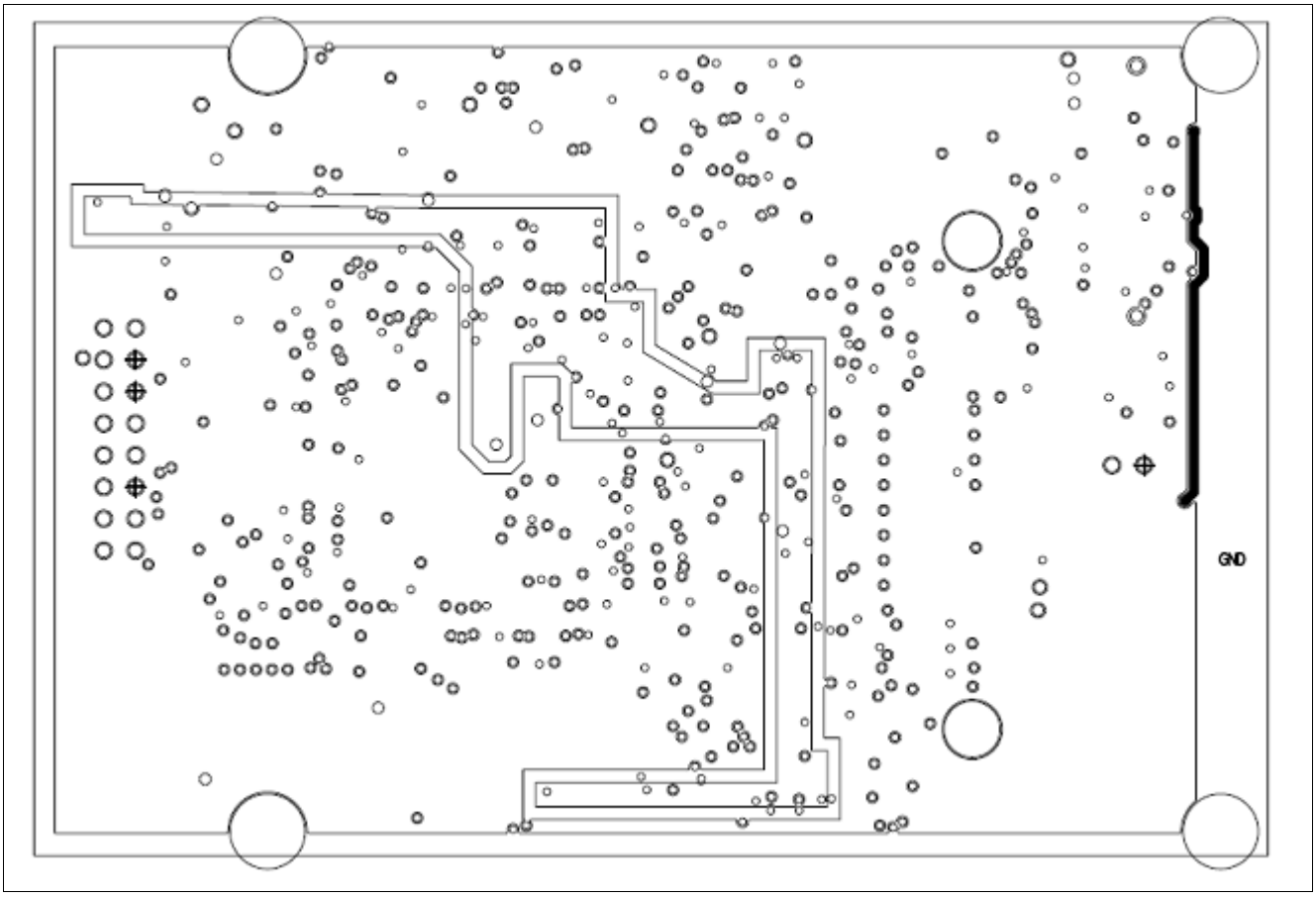


Figure 84 Logic Board v1.2 - Layer 2

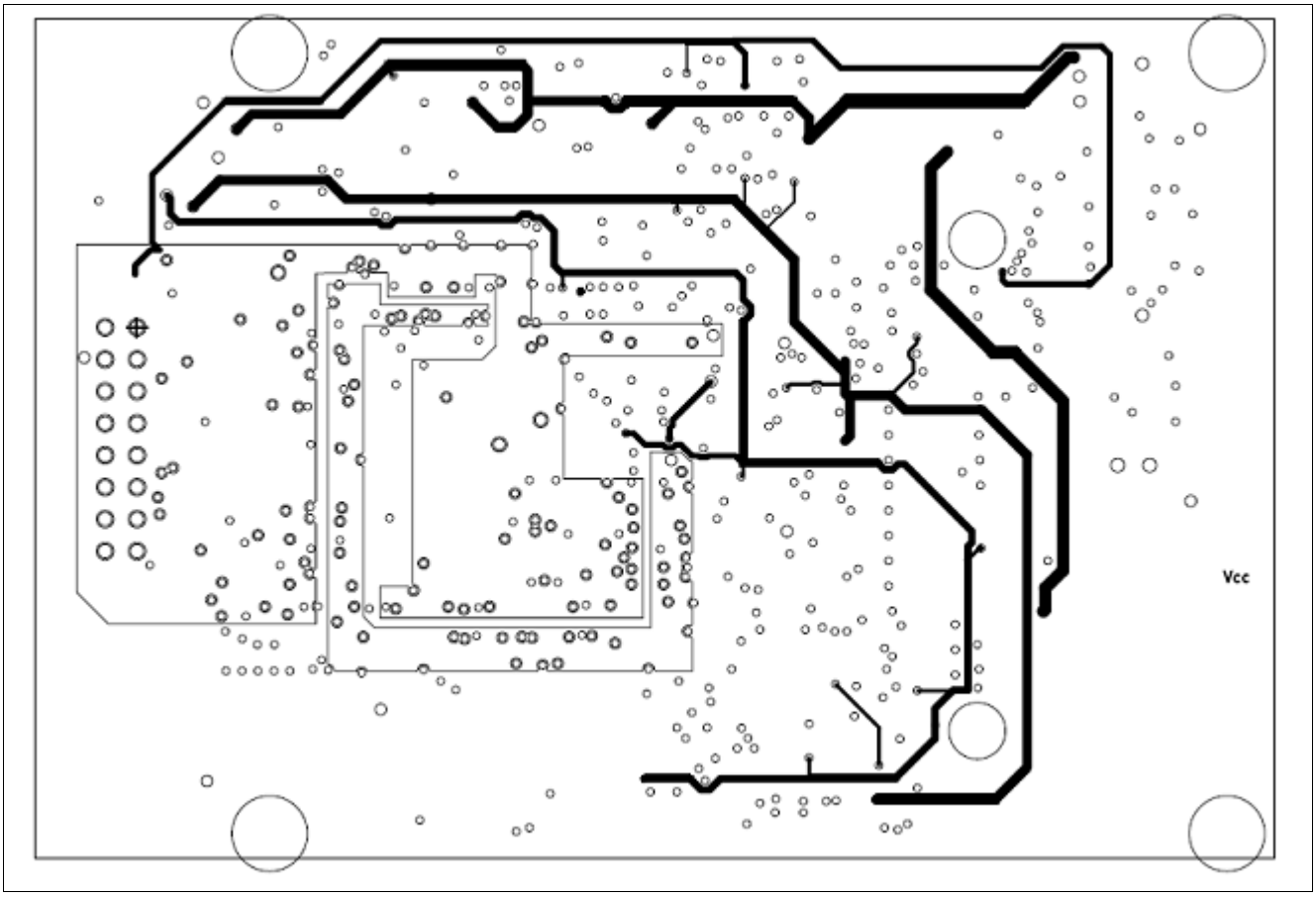


Figure 85 Logic Board v1.2 - Layer 3

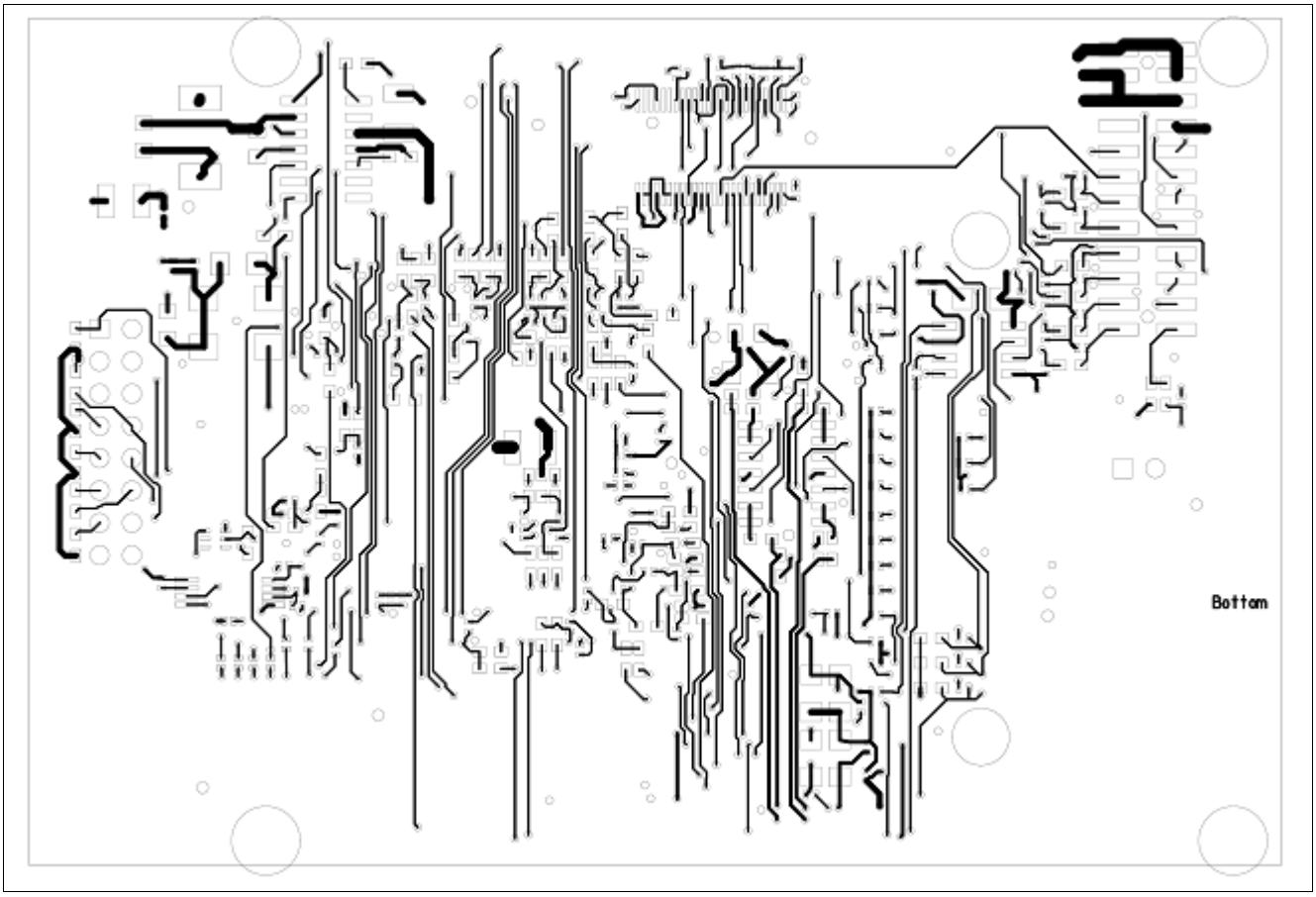


Figure 86 Logic Board v1.2 - Bottom Layer

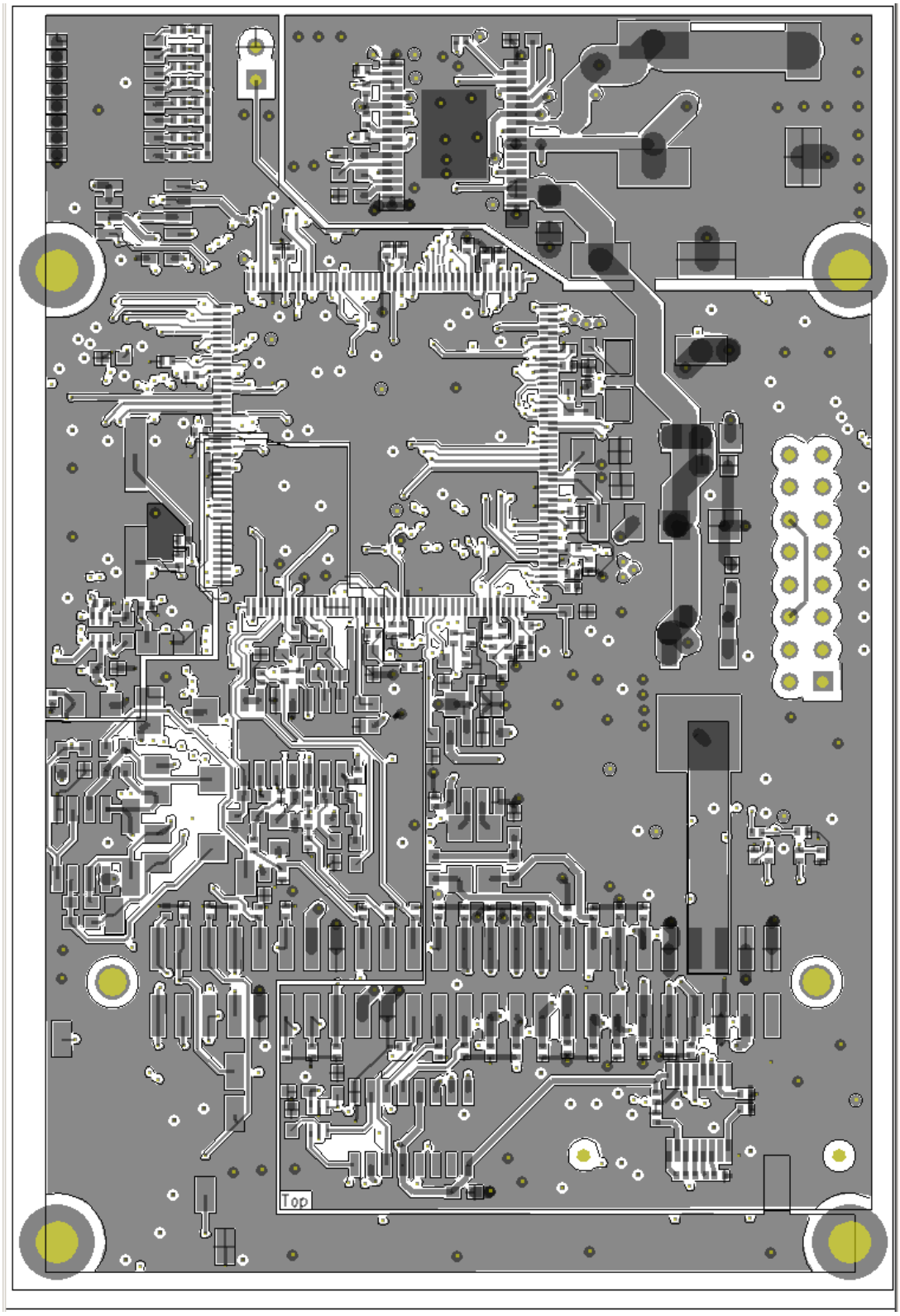


Figure 87 Logic Board v1.3b - Top Layer

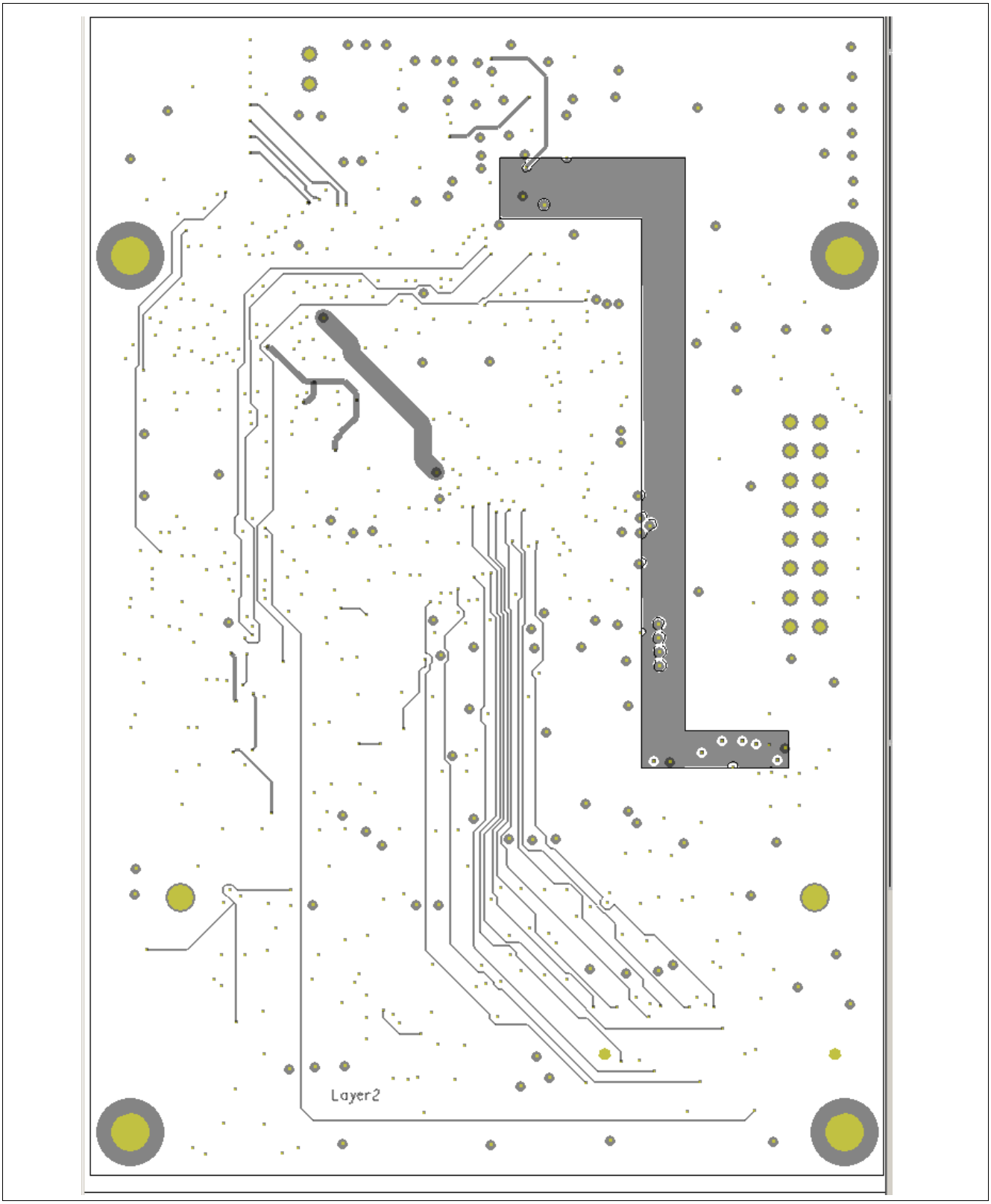


Figure 88 Logic Board v1.3b - Layer 2

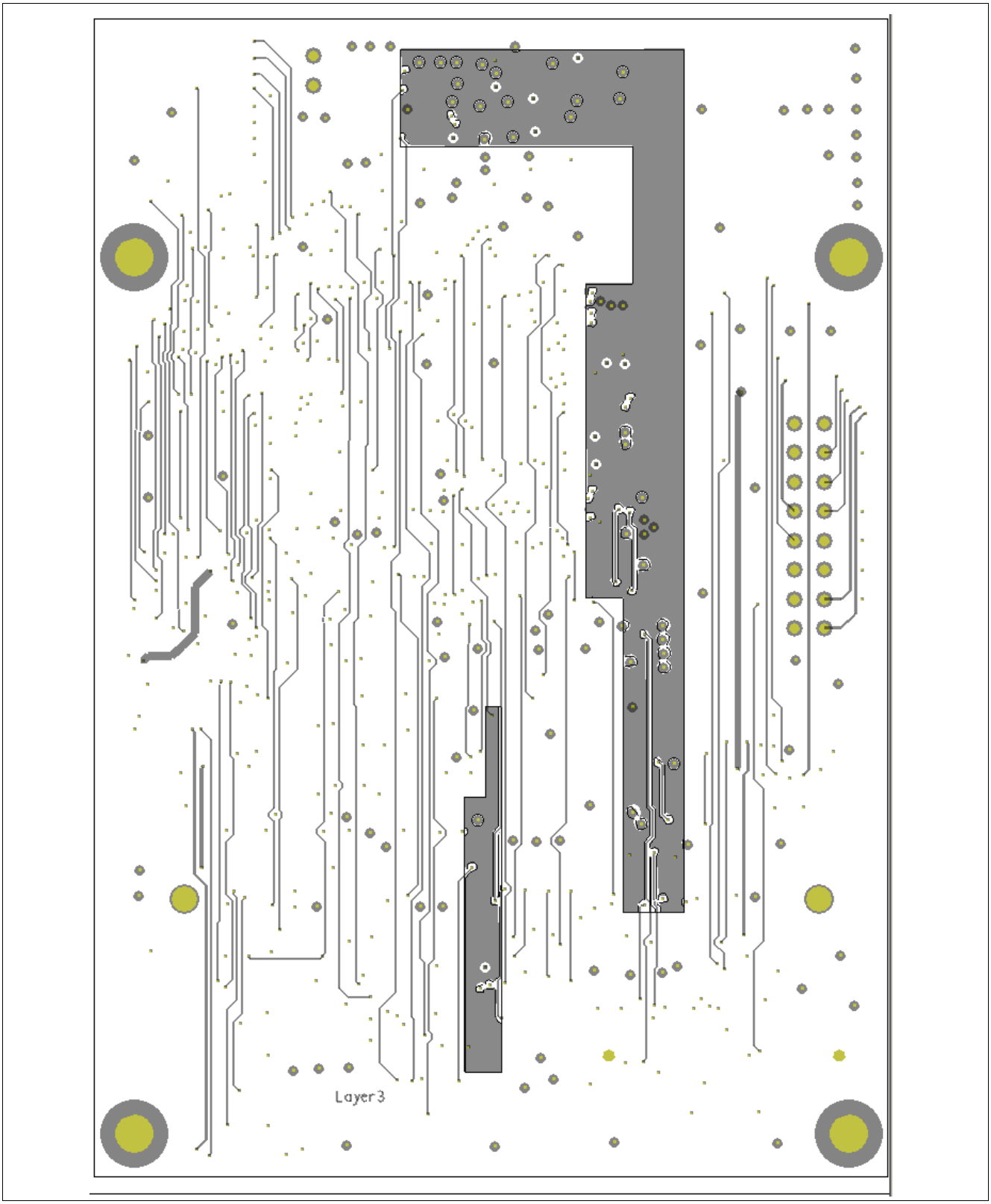


Figure 89 Logic Board v1.3b - Layer 3

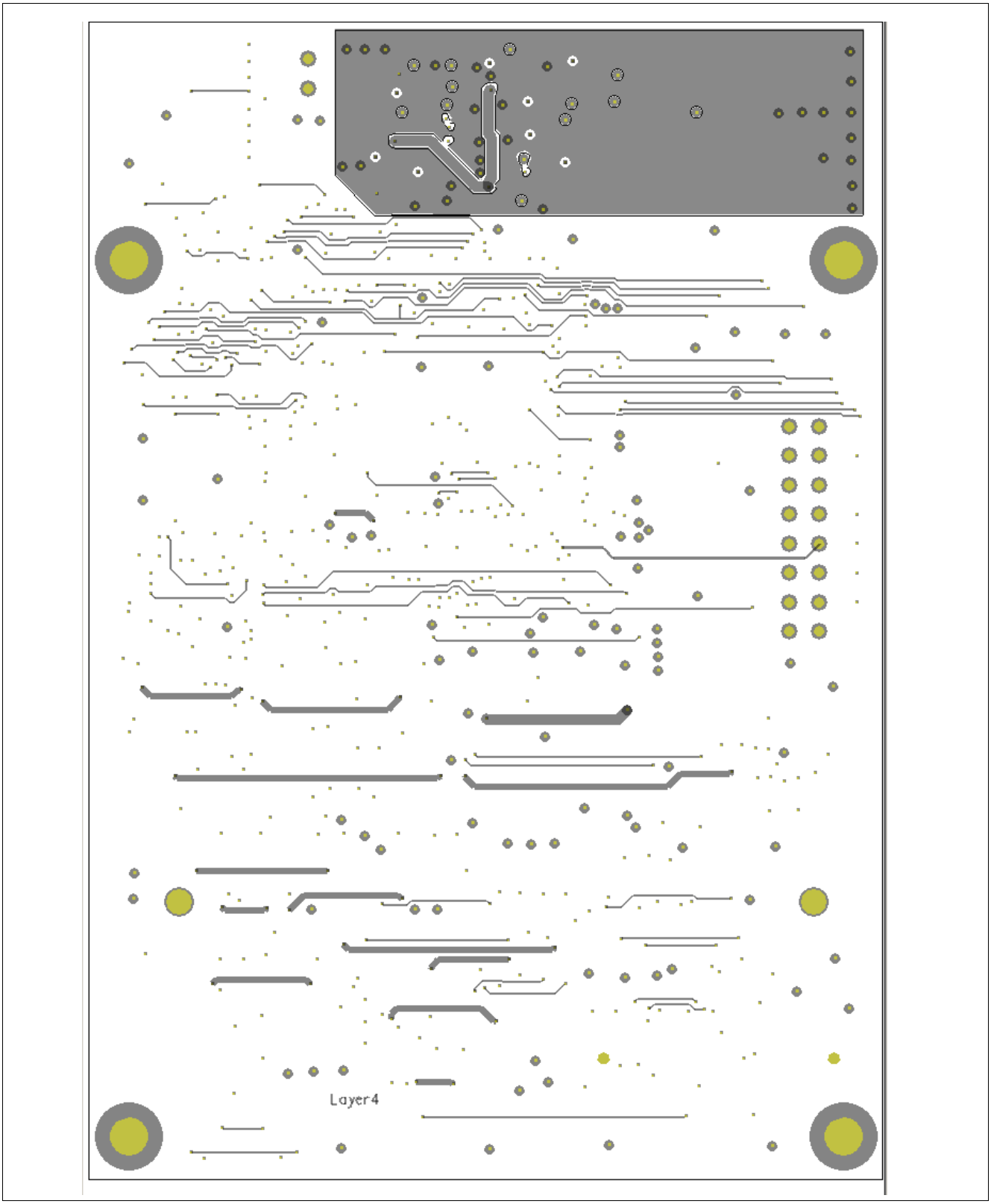


Figure 90 Logic Board v1.3b - Layer 4

Figure 91 Logic Board v1.3b - Layer 5

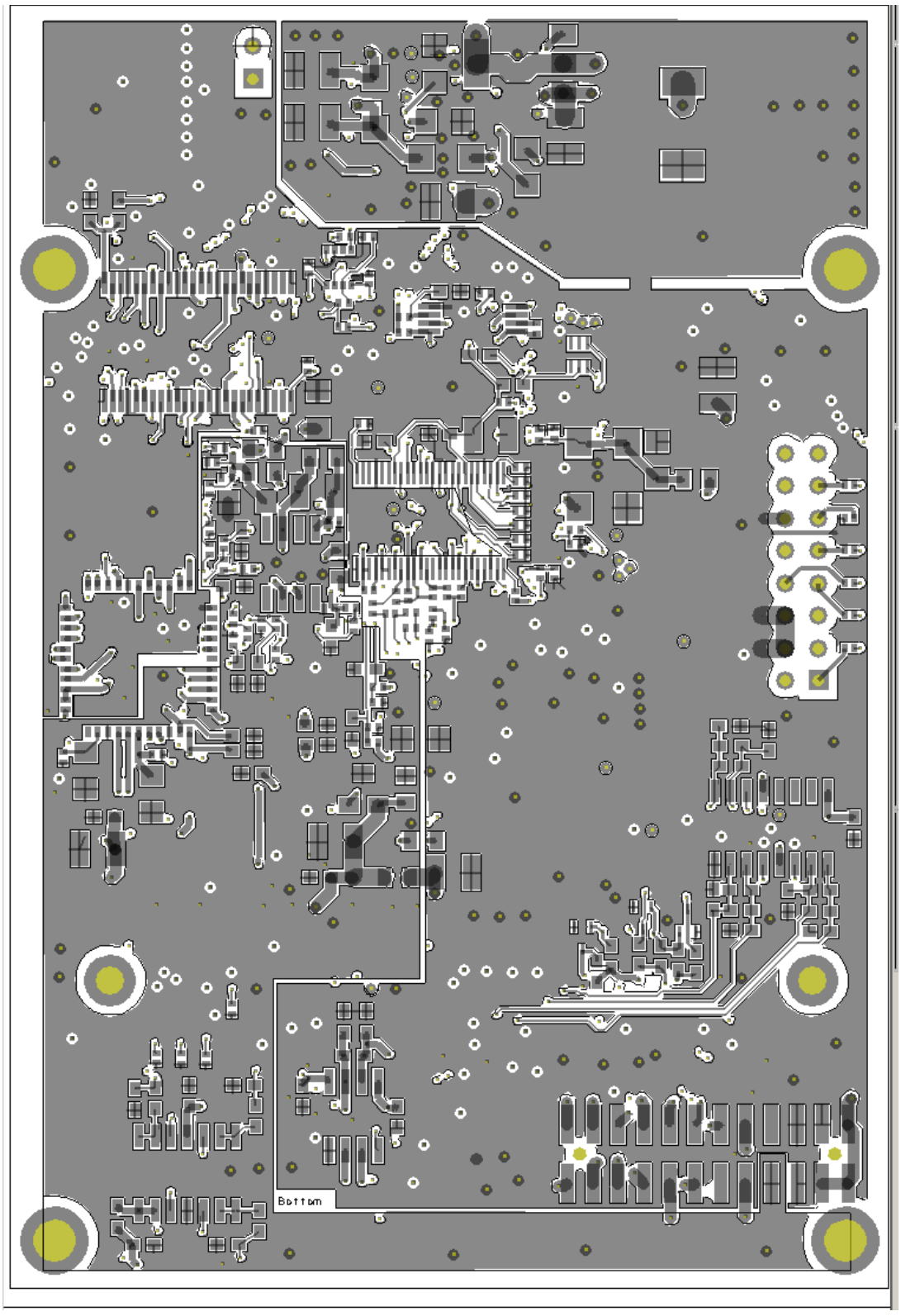


Figure 92 Logic Board v1.3b - Bottom Layer

4.12.4 Bill of Materials

Table 8 Bill of Materials for Hybrid Kit for the HybridPACK™2 Logic Board v1.2

Reference	Value / Device	Package
C1,C2,C3,C4,C5,C6,C7,C8,C9,C10,C13,C14, C15,C16,C17,C18,C19,C23,C24,C25,C26,C27 , C28	10n/50V/X7R	C0402
C29,C64,C65,C66,C68,C70,C71,C85,C87,C89 , C95,C98,C106,C107,C109,C111,C112,C113, C114,C115,C148,C149,C152,C153,C154,C15 5,C156,C157,C158,C159,C160,C163,C164,C1 65,C166,C167,C168,C169,C170,C171,C1110	100n/16V/X7R	C0402
C60,C61,C62,C63,C67,C69	100pF/50V/COG	C0402
C75	4u7/16V/X7R	C1206
C76,C77,C80,C81,C104	10n/16V/X7R	C0402
C78,C88,C90	10uf/10V/X7R	C1206
C79,C82	4u7/25V/X7R	C1206
C83,C84	20pF/50V/COG	C0402
C86	22u/16V/X7R	C1210
C91,C92	220nF/50V/X7R	C0805
C93	100uF/35V	C1010
C94	100uF/10V	C3528
C96	2.2nF	C0402
C97	10uF/6.3V/X7R	C1206
C105,C108	22uF/6.3V/X7R	C1206
C110	4.7n/50V/X7R	C0603
C143,C1111	22uF/16V/X7R	C1210
C144,C1112	100n/25V/X7R	C0603
C145,C146,C147,C161,C162	47n/16V/X7R	C0402
C150,C151	10uF/6.3V	C3216
C172,C173,C174,C175,C176,C177,C178,C17 9,C180,C181,C182,C183,C184,C185,C186,C1 87,C189,C191,C193,C194,C196,C198,C199,C 200,C201	100p/50V/X7R	C0402
D1	MBRS340T3	SMC
D2	BZV55/C13	SOD80
D3	1SMB30AT3	SMB
D4	LED_LSM676-MQ	L0805
FL1	B82789C0104N001	B82789C0
J1	Jumper	
K1	TW-12-06-L-D-475-SM-A	12POL

Table 8 Bill of Materials for Hybrid Kit for the HybridPACK™2 Logic Board v1.2 (cont'd)

Reference	Value / Device	Package
L1,L2,L5,L8	MURATA_BLM21P221SN	L0805
L3	47uH/B82464G4473M	B82464G4
L6,L7	B82422A1103K	C1210
Q1	SPD09P06PLG	TO252-3
Q2,Q3	BC847BL3	TSLP3-1
Q4	IPD90P03P4L-04	TO252-003
Q6	BCR183S	SOT363
R1,R2,R3,R4,R5,R6,R101,R115,R116,R118, R122,R128,R169,R174,R177,R186,R195	10K	R0603
R7,R8,R9,R71,R73,R173	10K	R0402
R10	opt	R0402
R72,R87,R89,R91,R94,R97	100R	R0603
R74,R75,R76,R77,R78,R79,R80,R81,R82,R83 , R84,R85,R86,R88,R165	1K	R0402
R90,R93,R96,R99	15K	R0603
R92,R95,R98,R100,R134,R135	1K	R0603
R102,R104,R106,R108,R121,R224,R316	0R	R0603
R103,R105,R107,R109,R110,R149,R154,R17 6,R181,R185,R192,R194,R202,R203,R208,R2 17,R228,R235,R236	opt	R0603
R111	20K	R0603
R112	39K	R0603
R113	0R	R1210
R114	47mR/0.33W	R0805
R119	680R	R0603
R131,R132	60R	R0603
R133	5K1	R0603
R150,R151,R153,R171	4K7	R0603
R155,R156,R157,R158,R159,R160	opt	R0603
R161,R162,R163,R164,R166,R167,R168	680R	R0402
R170,R229,R315	0R_opt	R0603
R172	220R	R0603
R175,R178,R179,R180,R184,R187,R188,R18 9,R191,R196,R197,R198,R199,R204,R205,R2 06,R213,R214,R222,R223,R230,R231,R234,R 238,R240	51K	R0603
R182,R183,R190,R193,R200,R201,R207,R21 0,R216,R227,R237,R239,R241	91K	R0603
SW1	Tyco_1-1571983-1	DIP
U1	AT25256A-10TQ-2.7	TSSOP-08

Table 8 Bill of Materials for Hybrid Kit for the HybridPACK™2 Logic Board v1.2 (cont'd)

Reference	Value / Device	Package
U2	74ALVC164245DGG	TSSOP-48
U4	LT1639HS	SO-14
U6	LMH6672	SO8
U8	AD2S1200YST	LQFP-44
U9	74LVC1G04GW	SOT353
U11	HCM49 8.192MABJ-UT	HCM49
U12	TPS76733QD	SO8
U13	TLE6389-2GV50	P-DSO-14
U14	TPS76715QD	SO8
U16	EH2645ETTTS-20.000M	SM_Q_EH26
U17	TLE6250GV33	SO8
U18	MAX3232EIPWRQ1	TSSOP-16
U23	MAX6369KA-T	SOT23-8
U24	SAK-TC1767-256F133HL	LQFP-176
U25	TLE4266GSV10	SOT223-4
X1-SIG1	Harwin M80-5123442	34POL
X3-OCDS1	HEADER 8X2	16POL
U58	MAX6457UKD3A-T	SOT23-5

Table 9 Bill of Materials for hybrid Kit for HybridPACK™2 Logic Board v1.3b

Reference	Value / Device	Package
C29,C64,C68,C70,C71,C106,C107,C109,C111,C112,C113,C114,C115,C123,C148,C149,C152,C153,C154,C155,C156,C157,C158,C159,C160,C161,C163,C164,C165,C166,C167,C168,C169,C170,C171,C1110,C1210	100n/16V/X7R	C0402
C65,C66,C1127,C1129,C1131,C1132,C1133,C1160,C1161,C1163,C1164	100n/16V/X7R	C0603
C75	4u7/16V/X7R	C1206
C76,C77,C80,C81,C104	10n/16V/X7R	C0402
C78	10uF/10V/X7R	C1206
C79,C82	4u7/25V/X7R	C1206
C83,C84	20pF/50V/COG	C0402
C85,C1151,C1153	100n/50V/X7R	C0603
C86,C1135,C1136,C1154,C1155	22u/16V/X7R/F_1463575	C1210
C92	220nF/100V/C3216X7R2A224KT5	C1206
C93,C1152	100uF_35V_MAL214097001E3	C1010_CAP_Pin1_Plus
C105,C108	22uF/6.3V/X7R	C1206

Table 9 Bill of Materials (cont'd)**for hybrid Kit for HybridPACK™2 Logic Board v1.3b**

Reference	Value / Device	Package
C110	4.7n/50V/X7R	C0603
C143,C1111	22uF/16V/X7R	C1210
C144	100n/25V/X7R	C0603
C145,C146,C147	47n/16V/X7R	C0402
C150,C151,C1157,C1158	10u/10V/X7R	C1206
C172,C173,C176,C178,C180,C183,C184,C187,C1169,C1170,C1171,C1173,C1174,C1175,C1176,C1177,C1178,C1179,C1180,C1183,C1184,C1185,C1189,C1190,C1191,C1192,C1193,C1194,C1195,C1196,C1197	1n/50V/X7R	C0402
C174,C179,C182	100p/50V/X7R	C0402
C191,C194,C196	6800p/10V/C0G	C0603
C1040,C1041,C1042,C1043,C1044,C1045,C1147,C1148,C1149	10p/50V/X7R	C0603
C1064,C1065,C1067	3300p/10V/C0G	C0603
C1112,C1167	100n/50V/X7R/C0805F104K5	C0805
C1128,C1130	10p/16V/X7R	C0603
C1142	4u7/10V/X7R	C1210
C1144,C1146	4u7/10V/X7R/F_9402195	C1206
C1145	1u/25V/X7R/F_1637035	C0603
C1150	680n/50V/F_1414702	C1206
C1156	220n/25V/X7R/F_1414626	C0603
C1159	1n/16V/X7R	C0402
C1166	4.7u/50V/X7R/C1210F475K5	C1210
C1172,C1181,C1182,C1187,C1188,C1201,C1202,C1203,C1204,C1205,C1206,C1207,C1208,C1209	1n/50V/X7R_opt	C0402
C1211	100n/50V/X7R	C0805
C1212	22n/50V/X7R	C0603
R10,R103,R105,R107,R109,R110,R176,R181,R185,R192,R194,R202,R203,R208,R477,R480,R481,C1213,C1214,C1215,C1216,C1217	opt	R0603
D1	MBRS340T3	SMC
D2	BZV55/C13	SOD80C_Pin1_Cathode
D3	1SMB30AT3	SMB
D4	LED_LSM676-MQ	Vishay_TLMK2300
D5,D6	SS12_1A_If_20V_Vr	DO214AC_SMA_Pin1_Cathode
D7,D8,D9	BAT54-04W	SOT323
FL1	B82789C0104N001	EPCOS_B82789C0

Table 9 Bill of Materials (cont'd)**for hybrid Kit for HybridPACK™2 Logic Board v1.3b**

Reference	Value / Device	Package
IC1	AT25256A-10TQ-2.7	TSSOP8
IC2	74ALVC164245DGG	TSSOP48
IC4,IC31	LT1639HS	SO14
IC6	LMH6672	SO8
IC8	AD2S1200YST	LQFP44_P0_8
IC13	TLE7368E	SO36-38
IC16	EH2645ETTTS-20.000M	Ecliptek_EH2645
IC17	TLE6250GV33	SO8
IC23	MAX6369KA-T	SOT23-8
IC24	SAK-TC1767-256F133HL	LQFP176_p0_50
IC25	TLE4266GSV10	SOT223
IC26	DS92LV010	SO8
IC28,IC30	74LVC2G04GW	SOT363
IC29	74LVCH16T245DL	SSOP48
IC32	DS90LV031A	SO16-1
IC33	AM26C32QD	SO16-1
IC52	MAX3232EIPWRQ1	TSSOP16
IC53	MAX6143AASA50	SO8
IC54	LM50CIM3	SOT23
J1	Jumper	jumper_2way
K1	TW-12-06-L-D-475-SM-A	Samtec_TW-12-06-L-D-475-SM-A
K2	Harwin M80-5125042P	Harwin_M80-5125042P
K3-OCDS	HEADER 8X2	tyco_1761686-6
L1,L8,L9,L10,L11,L12	MURATA_BLM21PG221SN	L0805
L3	WE_7447709470	WE-PD_744770
L5	MURATA_BLM21P221SN	L0805
L6,L7	B82422A1103K	L1210
Q2	BDP949	SOT223
Q4	IPD90P03P4L-04	TO252-3
Q6	BCR183S	SOT363
R1,R2,R3,R4,R5,R6,R7,R8,R9,R71,R73, R173,R174,R177,R186,R195,R471,R473, R474,R475,R476	10K	R0402
R74,R75,R76,R77,R78,R79,R80,R88,R92, R95,R98,R100,R134,R135,R161,R162,R163, R164,R165,R166,R167,R168,R180,R187, R197,R234,R238,R240,R456	1K	R0402
R90,R93,R96,R99	15K	R0402
R101,R128,R169	10K	R0603

Table 9 Bill of Materials (cont'd)**for hybrid Kit for HybridPACK™2 Logic Board v1.3b**

Reference	Value / Device	Package
R102,R104,R106,R108,R478,R479,R482,R497	0R	R0603
R113	SMK-R000 / Isabellenhuette	R1206
R131,R132	60R	R0603
R133	5K1	R0402
R149,R154	opt	R0402
R150,R151,R153	4K7	R0402
R155,R156,R158,R160	2K4/0.1%	R0603
R157	390/0.1%	R0603
R159	3K3/0.1%	R0603
R170,R224,R498	0R_opt	R0603
R171	4K7	R0603
R172	220R	R0603
R175,R184,R191,R198,R205	68K	R0402
R178,R179,R188,R189,R196,R199	51K	R0402
R182,R193,R200	91K	R0402
R183,R190,R201,R237,R239,R241	2K	R0402
R214,R217,R223,R228,R230,R235	6K8	R0402
R215,R218,R472	3K3	R0402
R229	0R	R0402
R429,R430,R431,R447	100R	R0603
R483,R484,R485	5K_pot_0,25W_20%_Bourns_3314J_opt	Bourns_3314J
R486	0R / 0.1%	R0402
R487	270K	R0603
R488,R489,R490,R494,R495,R496	1K	R0603
R491,R492,R493	2K7	R0603
R499,R500,R501,R502,R503,R504,R505, R506	100k	R0402
SW1	Tyco_1-1571983-1	Tyco_1-1571983-1
SW2	SW DIP-4/SM	SO8
TP1,TP2,TP3,TP4,TP5,TP6,TP7,TP8,TP9	Testpad_SMD_Ettinger	Ettinger_12_18_815_testpad
U1	HCM49 8.192MABJ-UT	Citizen_HCM49

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